OSCILLATORS

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1 INTRODUCTION

Modern communications systems need oscillators as part of the design. In most cases, these oscillators are part of a synthesizer and they are voltage controlled, meaning that the frequency is determined by tuning diodes, frequently called varactors. The applied direct current(DC) voltage varies the frequency. For high-performance circuits, the Colpitts oscillator is most frequently selected [1–34].

The Colpitts oscillator comes in three flavors—Fig. 1a shows the conventional circuit configuration. This type of circuit is based on a design developed by Edwin Henry Colpitts known for his invention of this oscillator and, hence, carries his name [1]. It uses a capacitive voltage divider and an inductor. In reality, this simple circuit is not used but rather a derivation of this. This is shown in Fig. 1b. The advantage of this circuit is that the values for C_1 and C_2 are fixed and the change in frequency occurs by changing C_3. If the frequency of Fig. 1a needs to be changed, a better choice is to vary the inductor L.

His colleague Ralph Hartley [2] invented an inductive coupling oscillator. The advantage of such an oscillator having capacitors C_1 and C_2 replaced with a tap of the inductor has been used together with helical resonators. The frequency tuning is achieved purely capacitively. To minimize loading, the transistor of choice here is a field effect transistor (FET) which has very high input impedance and provides minimum loading to the circuit. The disadvantage is that this circuit, using junction FETs, is limited to about 400 MHz. The transition frequency f_T is about 500 MHz. FETs can also be used in the Colpitts oscillator as shown in Fig. 1a, because of relatively lower loading than the bipolar transistor. The drawback of Fig. 1a is the heavy loading of the tuned circuit by the transistor. The circuit shown in Fig. 1b is frequently referred to as the Clapp–Gouriet circuit [3].

At frequencies below 1 GHz, both Gallium, arsenide (GaAs) FETs and complementary metal-oxide semiconductor (CMOS) FETs are not a good choice because of their high flicker noise contribution.

For the circuit of Fig. 1b, it is theoretically possible to have L and C_3 in resonance, in which case, the oscillator will cease to work. It is important to note here that the same circuit is used also for crystal oscillators; here, the inductor L is replaced by the crystal. The crystal is a series combination of L_s, R_s, and C_s with $Q = \omega L/R$. In practice, the product of crystal Q and frequency is a constant. For 5 MHz, a typical Q of 2.5×10^6 is possible, resulting in a product of 12.5×10^{12}. If this is scaled to a crystal oscillator operating at 100 MHz, the Q would be 125,000. Manufacturers typically guarantee values greater than 100,000.
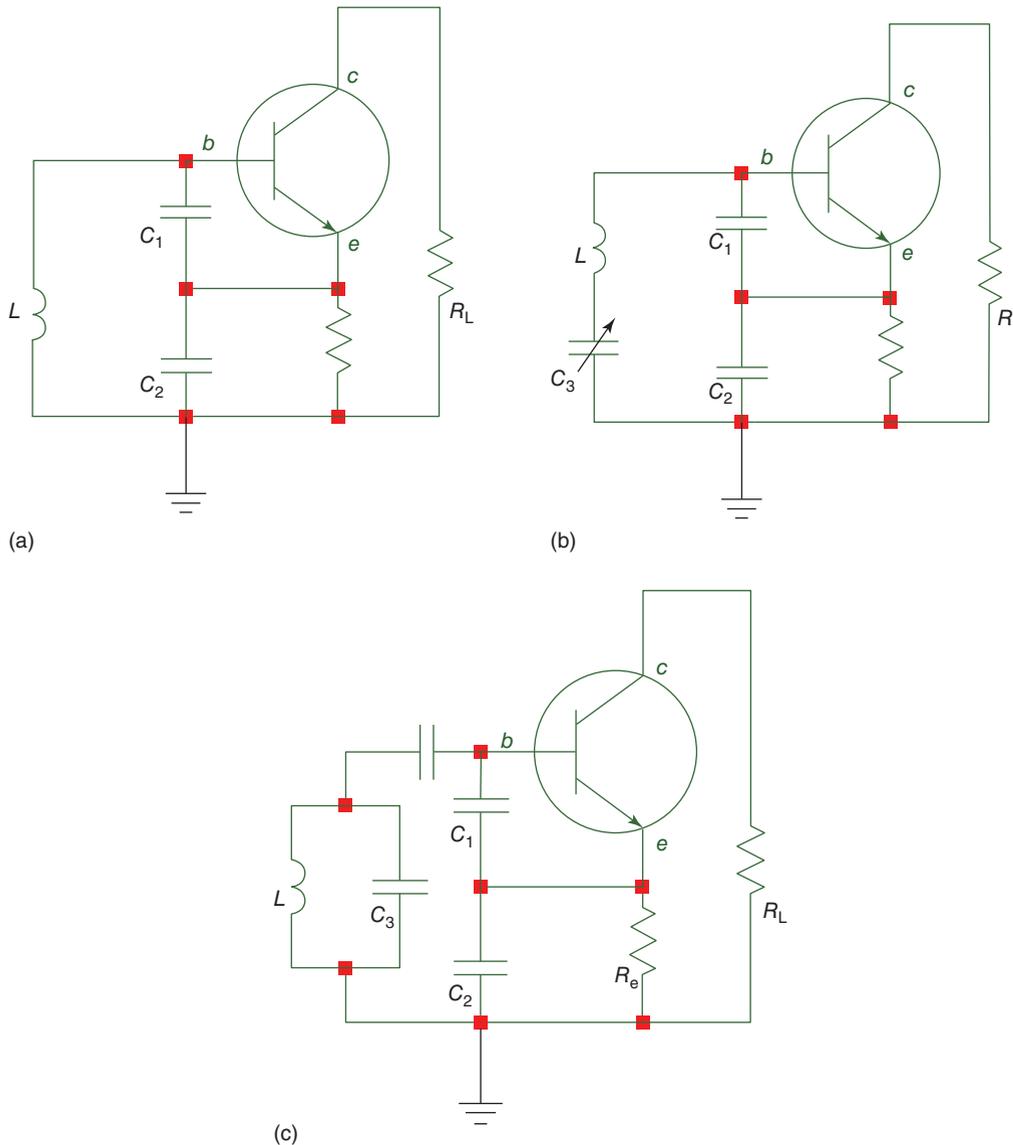
Figure 1 (a) Conventional Colpitts configuration. (b) Modified Colpitts (Clapp–Gouriet) config. (c) Modified Colpitts oscillator (Rohde and Apte [33]/IEEE).

Again, this crystal oscillator also falls into the category of Colpitts oscillator. A third variation is shown in Fig. 1c. Here, we have a parallel-tuned circuit which is coupled loosely to the transistor. This circuit is found when building oscillators using ceramic resonators (CROs). Figure 2 shows such a design.

The following section summarizes the various methods of oscillator analysis and presents a step-by-step design procedure, showing the simulated, measured, and calculated results for phase noise and other important parameters and includes a discussion on the effect of tuning diodes.
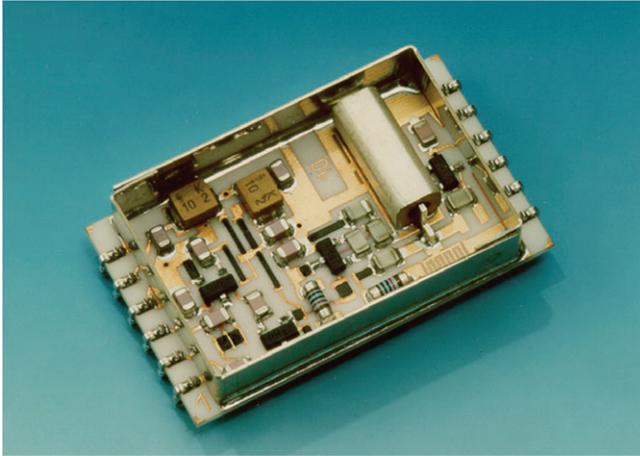
Figure 2 Photograph of 1 GHz CRO (Rohde [2]/John Wiley & Sons).

2   LINEAR APPROACH

For many years, until recently, oscillators were analyzed with a linear approach as will be shown below.[1] Figures 3a,b illustrates the oscillator sub-circuit for the purpose of calculating the negative resistance.

From Fig. 3b, the circuit equation is given from Kirchhoff's voltage law (KVL) as

$$V_{\text{in}} = I_{\text{in}}(X_{C_1} + X_{C_2}) - I_b(X_{C_1} - \beta X_{C_2}) \tag{1a}$$

$$0 = -I_{\text{in}}(X_{C_1}) + I_b(X_{C_1} + h_{ie}) \tag{1b}$$

Considering, $\frac{1}{Y_{11}} = h_{ie}$

$$Z_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{(1+\beta)X_{C_1}X_{C_2} + h_{ie}(X_{C_1} + X_{C_2})}{X_{C_1} + h_{ie}} \tag{1c}$$

$$Z_{\text{in}} = \frac{\left(-\frac{(1+\beta)}{\omega^2 C_1 C_2} + \frac{(C_1+C_2)}{j\omega C_1 C_2}\frac{1}{Y_{11}}\right)}{\left(\frac{1}{Y_{11}} + \frac{1}{j\omega C_1}\right)} \tag{1d}$$

The input impedance (Z_{IN}) of the Colpitts oscillator circuit, shown in Fig. 3c, including the parasitics are given as [4, 5]

$$Z_{\text{IN}}|_{\text{package}} = -\left[\frac{Y_{21}}{\omega^2(C_1+C_p)C_2}\frac{1}{(1+\omega^2 Y_{21}^2 L_p^2)}\right] - j\left[\frac{(C_1+C_P+C_2)}{\omega(C_1+C_P)C_2} - \frac{\omega Y_{21}L_P}{(1+\omega^2 Y_{21}^2 L_p^2)}\frac{Y_{21}}{\omega(C_1+C_P)C_2}\right] \tag{2}$$

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1 Note that the linear approach does not model *any* amplitude limiting mechanism. The consequence is that the predictions made by this approach are limited to very small amplitudes (or the startup phase). We will come back on this remark later.
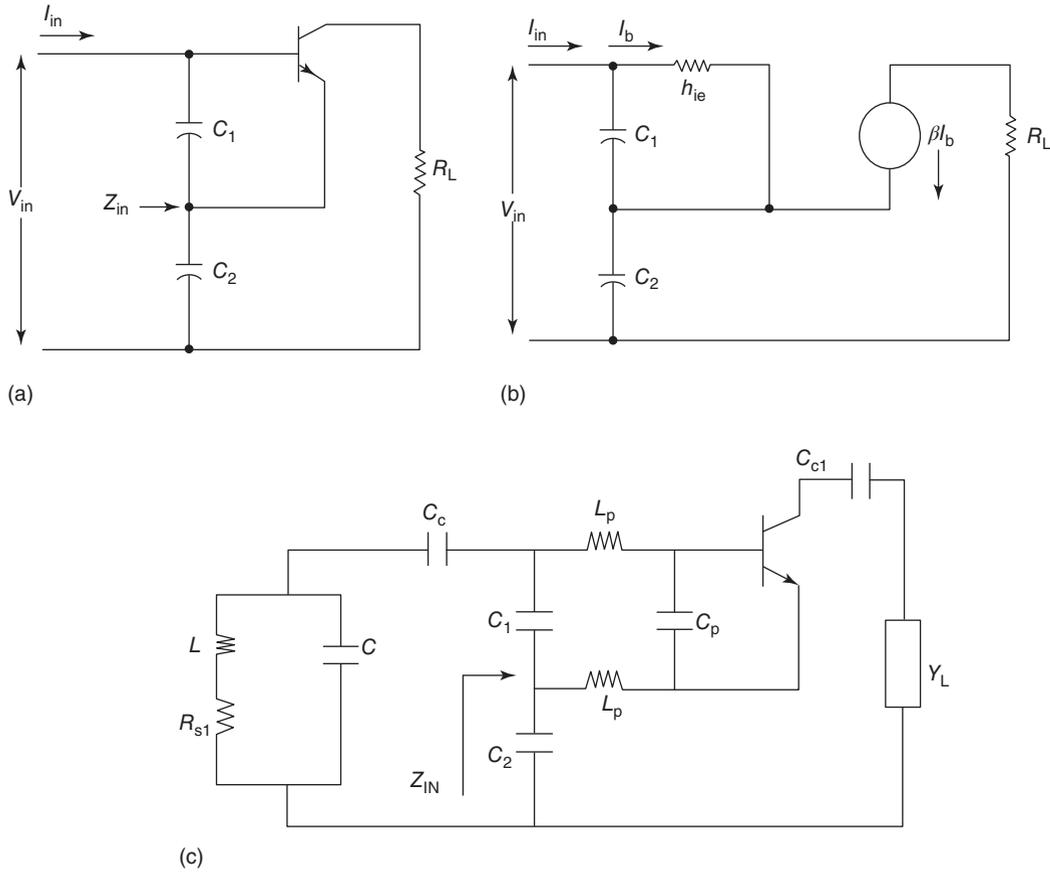
Figure 3 (a) Oscillator sub-circuit for impedance analysis. (b) Equivalent sub-oscillator circuit for the calculation of the negative resistance. (c) Colpitts oscillator with base lead inductances and package capacitance (Rohde et al. [5]/John Wiley & Sons).

The resonator losses are expressed by the R_{s1}. Now, by splitting the Z_{IN} of the Colpitts oscillator into real and imaginary parts, including parasitics, we obtain,

$$R_{\text{NEQ}} = \frac{R_{\text{N}}}{\left(1 + \omega^2 Y_{21}^2 L_P^2\right)} \tag{3}$$

$$\frac{1}{C_{\text{EQ}}} = \left\{ \left[\frac{1}{\frac{(C_1 + C_P)C_2}{(C_1 + C_2 + C_P)}} \right] - \left[\frac{\omega^2 Y_{21} L_P}{\left(1 + \omega^2 Y_{21}^2 L_P^2\right)} \right] \left[\frac{Y_{21}}{\omega(C_1 + C_P)C_2} \right] \right\} \tag{4}$$

$$R_{\text{N}} = -\frac{Y_{21}}{\omega^2 C_1 C_2} \tag{5}$$

where

R_{N} is the negative resistance without lead inductance and package capacitance;

R_{NEQ} is the negative resistance with base-lead inductance and package capacitance;

C_{EQ} is the equivalent capacitance with base-lead inductance and package capacitance.
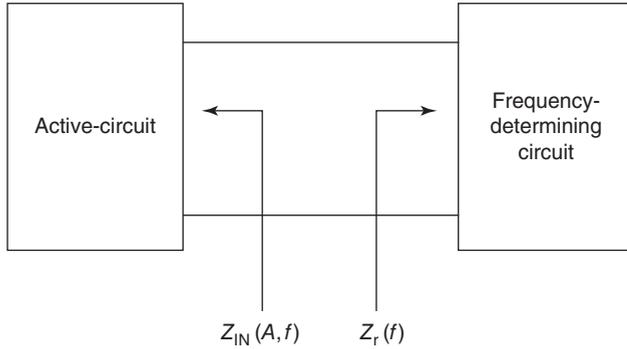
Figure 4 Schematic diagram of a one-port negative resistance model (Rohde et al. [5]/John Wiley & Sons).

The method shown above is called one-port oscillator design [6]. Figure 4 shows the general schematic diagram of a one-port negative-resistance model. The negative real part of Z_{IN} is used to compensate the losses of the parallel-tuned circuit.

3   LINEAR S-PARAMETERS APPROACH

It may be interesting for the readers to see how an oscillator can be analyzed using *S*-parameters. It should be noted that this method is based on linear approximations and works for practically all microwave oscillator designs [6, 28, p. 741]. The equivalent criteria of the negative resistance can be calculated in the form of *S*-parameters. The detailed definitions of *S*-parameters can be found in [31]. This negative resistance will cause oscillations if the following conditions are satisfied. Assume that the oscillation condition is satisfied at port 1 and is given by

$$\frac{1}{S'_{11}} = \Gamma_G \tag{6}$$

Thus,

$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{S_{11} - D\Gamma_L}{1 - S_{22}\Gamma_L} \tag{7}$$

$$\frac{1}{S'_{11}} = \frac{1 - S_{22}\Gamma_L}{S_{11} - D\Gamma_L} = \Gamma_G \tag{8}$$

From expanding (7), we get

$$\Gamma_G S_{11} - D\Gamma_L \Gamma_G = 1 - S_{22}\Gamma_L \tag{9}$$

$$\Gamma_L(S_{22} - D\Gamma_G) = 1 - S_{11}\Gamma_G \tag{10}$$

$$\Gamma_L = \frac{1 - S_{11}\Gamma_G}{S_{22} - D\Gamma_G} \tag{11}$$

$$S'_{22} = S_{22} + \frac{S_{12}S_{21}\Gamma_G}{1 - S_{11}\Gamma_G} = \frac{S_{22} - D\Gamma_G}{1 - S_{11}\Gamma_G} \tag{12}$$

$$\frac{1}{S'_{22}} = \frac{1 - S_{11}\Gamma_G}{S_{22} - D\Gamma_G} \tag{13}$$

Comparing Eqs. (9) and (12), we find that

$$\frac{1}{S'_{22}} = \Gamma_G \tag{14}$$

where S_{11} and S_{22} are the input and output reflection coefficients, respectively.

The discussion above means that the oscillation condition is also satisfied at port 2, which proves the simultaneous oscillation condition at both ports. Thus, if either port is oscillating, the other port must be oscillating as well. A load may appear at either or both ports, but normally the load is in Γ_L, the output termination.

It is helpful to use the common-source-based amplifier to compute the oscillator output power. For oscillators, the objective is to maximize $(P_{out} - P_{in})$ of the amplifier, which is the useful power to the load. An empirical expression for the common-source amplifier output power found by Johnson [29] is

$$P_{out} = P_{sat} \left(1 - \exp \frac{-GP_{in}}{P_{sat}} \right) \tag{15}$$

where P_{sat} is the saturated output power of the amplifier and G is the tuned small-signal common-source transducer gain of the amplifier, which is identical to $|S_{21}|^2$. Since the objective is to maximize $(P_{out} - P_{in})$, (where P_{out} and P_{in} are the output and input power of the amplifier, respectively),

$$d(P_{out} - P_{in}) = 0 \tag{16}$$

$$\frac{\partial P_{out}}{\partial P_{in}} = 1 \tag{17}$$

$$\frac{\partial P_{out}}{\partial P_{in}} = G_{exp} - \frac{GP_{in}}{P_{sat}} = 1 \tag{18}$$

$$\exp \frac{GP_{in}}{P_{sat}} = G \tag{19}$$

$$\frac{P_{in}}{P_{sat}} = \frac{\ln G}{G} \tag{20}$$

At the maximum value of $(P_{out} - P_{in})$, the amplifier output is

$$P_{out} = P_{sat} \left(1 - \frac{1}{G} \right) \tag{21}$$

And, the maximum oscillator output power is

$$P_{osc} = (P_{out} - P_{in}) \tag{22}$$

$$= P_{sat} \left(1 - \frac{1}{G} - \frac{\ln G}{G} \right) \tag{23}$$

Thus, the maximum oscillator output power can be predicted from the common-source amplifier-saturated output power and the small signal common-source transducer gain G. For high oscillator output power, high (loop) gain is of importance. Another definition of gain that is useful for large-signal amplifier or oscillator design is the maximum efficient gain and defined by

$$G_{ME} = \frac{P_{out} - P_{in}}{P_{in}} \tag{24}$$

For maximum oscillator power, the maximum efficient gain from (20) and (21) is

$$G_{MEmax} = \frac{G - 1}{\ln G} \tag{25}$$

The radio frequency (RF) gain G_{MEmax} is a considerably smaller value compared to G, the small-signal gain [7–12].

Designing oscillators based on S-parameters in a linear mode has been quoted by many authors using first approximation for large signal as shown in [8]. The problem with this published approach is that it uses a GaAs FET, where only the transconductance g_m has a major influence. S_{11} changes very little under large-signal conditions, as does S_{22}. Reliable large-signal S-parameters for bipolar transistors and FETs are difficult to get and only make sense if the surrounding circuitry is included in the model.

4 TIME-DOMAIN-BASED ANALYSIS TO ANALYZE THE TRANSISTOR NONLINEARITIES

A correction for the frequency-dependent parameters will follow, based on "simulation" for larger drive level. We will show how the derivations are made, and where problems arise and the domain where our assumptions are valid is no longer guaranteed.

The voltage $v(t)$ across the base–emitter junction consists of a DC component and a driven signal voltage $V_1 \cos(wt)$. It can be expressed as

$$v(t) = V_{\text{dc}} + V_1 \cos(wt) \tag{26}$$

This formula is a rather coarse approximation and does not include saturation, the early effect and base-emitter (BE) breakdown. Nevertheless, we will assume the validity of the formula above for the moment and come back to recheck it later.

As the driven voltage $V_1 \cos(wt)$ increases and develops enough amplitude across the base–emitter junction, the resulting current is a periodic series of pulses whose amplitude depends on the nonlinear characteristics of the device and is given as

$$i_e(t) = I_s e^{\frac{qv(t)}{kT}} \tag{27}$$

$$i_e(t) = I_s e^{\frac{qV_{\text{dc}}}{kT}} e^{\frac{qV_1 \cos(wt)}{kT}} \tag{28}$$

$$i_e(t) = I_s e^{\frac{qV_{\text{dc}}}{kT}} e^{x \cos(wt)} \tag{29}$$

assuming $I_c \approx I_e \ (\beta > 10)$

$$x = \frac{V_1}{(kT/q)} = \frac{qV_1}{kT} \tag{30}$$

$i_e(t)$ is the emitter current and x is the drive level which is normalized to kT/q.

From the Fourier series expansion, $e^{x \cos(wt)}$ is expressed as

$$e^{x \cos(wt)} = \sum_n a_n(x) \cos(nwt) \tag{31}$$

$a_n(x)$ is a Fourier coefficient and given as

$$a_0(x)\big|_{n=0} = \frac{1}{2\pi} \int_0^{2\pi} e^{x \cos(wt)} d(wt) = I_0(x) \tag{32}$$

$$a_n(x)\big|_{n>0} = \frac{1}{2\pi} \int_0^{2\pi} e^{x \cos(wt)} \cos(nwt) d(wt) = I_n(x) \tag{33}$$

$$e^{x \cos(wt)} = \sum_n a_n(x) \cos(nwt) = I_0(x) + 2 \sum_1^{\infty} I_n(x) \cos(nwt) \tag{34}$$

$I_n(x)$ is the modified Bessel function.

$$\text{As } x \to 0 \Rightarrow I_n(x) \to \frac{(x/2)^n}{n!} \tag{35}$$

$I_0(x)$ are monotonic functions having positive values for $x \geq 0$ and $n \geq 0$; $I_0(0)$ is the unity, whereas all higher order functions start at zero.

The short current pulses are generated from the growing large-signal drive level across the base–emitter junction, which leads to strong harmonic generation [5, 27]. The advantage of this pulse performance is the reduction of phase noise, due to the smaller duty cycle of the transistor [4]. The emitter current represented above can be expressed in terms of harmonics as

$$i_e(t) = I_s e^{\frac{qV_{dc}}{kT}} I_0(x) \left[1 + 2 \sum_1^\infty \frac{I_n(x)}{I_0(x)} \cos(nwt) \right] \tag{36}$$

$$I_{dc} = I_s e^{\frac{qV_{dc}}{kT}} I_0(x) \tag{37}$$

$$V_{dc} = \frac{kT}{q} \ln \left[\frac{I_{dc}}{II_0(x)} \right] \Rightarrow \frac{kT}{q} \ln \left[\frac{I_{dc}}{I_s} \right] + \frac{kT}{q} \ln \left[\frac{1}{I_0(x)} \right] \tag{38}$$

I_s is the collector saturation current

$$V_{dc} = V_{dcQ} - \frac{kT}{q} \ln I_0(x) \tag{39}$$

$$i_e(t) = I_{dc} \left[1 + 2 \sum_1^\infty \frac{I_n(x)}{I_0(x)} \cos(nwt) \right] \tag{40}$$

Table 1 For T = 300 K, Data Are Generated at a Different Drive Level

Drive level (x)	Drive Voltage $\left(\left[\frac{kT}{q} \right] * x \right)$ (mV)	Offset Coefficient $\ln[I_0(x)]$	DC Offset $\frac{kT}{q}[\ln I_0(x)]$ (mV)	Fundamental Current $2[I_1(x)/I_0(x)]$	Second-Harmonic $[I_2(x)/I_1(x)]$
0.00	0.000	0.000	0.000	0.000	0.000
0.50	13.00	0.062	1.612	0.485	0.124
1.00	26.00	0.236	6.136	0.893	0.240
2.00	52.00	0.823	21.398	1.396	0.433
3.00	78.00	1.585	41.210	1.620	0.568
4.00	104.00	2.425	63.050	1.737	0.658
5.00	130.00	3.305	85.800	1.787	0.719
6.00	156.00	4.208	206.180	1.825	0.762
7.00	182.00	5.127	330.980	1.851	0.794
8.00	208.00	6.058	459.600	1.870	0.819
9.00	234.00	6.997	181.922	1.885	0.835
10.00	260.00	7.943	206.518	1.897	0.854
15.00	390.00	12.736	331.136	1.932	0.902
20.00	520.00	17.590	457.340	1.949	0.926

Source: Rohde et al. [5]/John Wiley & Sons.
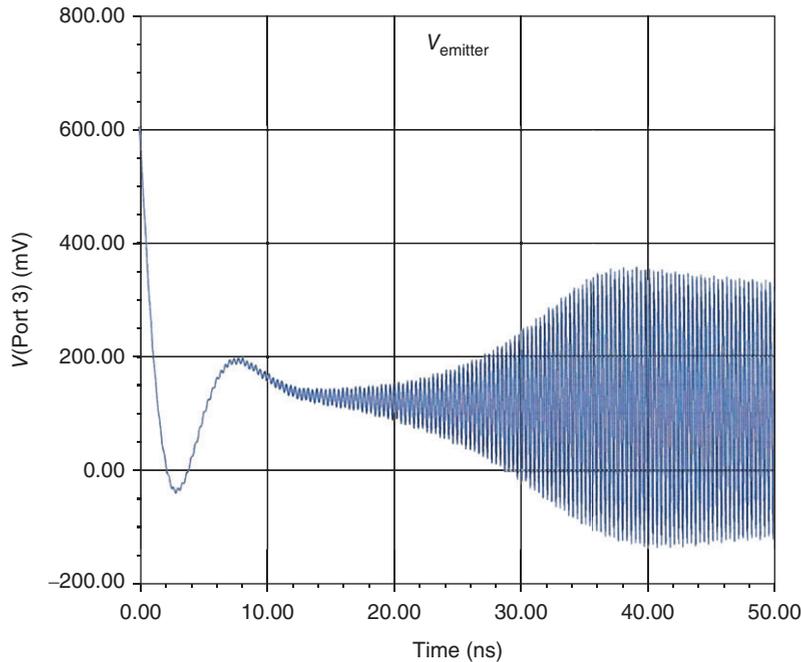
Figure 5 Example of the transient simulation of a ceramic resonator-based high-Q oscillator showing the DC offset as shown in column 4 of Table 1 (the voltage displayed is taken from the emitter) (Rohde et al. [5]/John Wiley & Sons).

$V_{\mathrm{dc}Q}$ and I_{dc} are the operating DC bias voltage and the DC value of the emitter current. Furthermore, the Fourier transform of $i_e(t)$, a current pulse, or series of pulses in the time domain yields a number of frequency harmonics common in oscillator circuit designs using nonlinear devices.

The peak amplitude of the harmonic content of the output current is defined as $\left[\frac{I_N(x)}{I_1(x)}\right]$, and the DC offset voltage is calculated analytically in terms of the drive level, as shown in Table 1. It gives good insight into the nonlinearities involved in the oscillator design.

It may be of interest to see the start-up condition of an oscillator; the transient response is shown in Fig. 5.

5 SELECTING THE RIGHT TRANSISTOR

The basic design of a Colpitts oscillator is the same, whether one uses a FET or bipolar junction transistor (BJT). Bipolar transistor-based oscillators can now easily be designed up to 20 GHz. The basic advantage of the bipolar transistor (also known as BIP) is the lower flicker noise corner frequency. Currently, transistor chips with F_{max} up to 300 GHz are available in the foundry environment, commercially up to about 150 GHz. For the purpose of this design synthesis, we have decided to use a BFG520, which is a highly linear transistor. It is validated with a 3-tone test (the typical 2-tone test is easier to meet), as found from the datasheet; the mixing products are better than −60 dB suppressed relative to the carrier. Based on past experience with its good linearity, the BFG520 also has low distortion and low noise. The key parameters are $V_{\mathrm{CEO}} = 15$ V, $I_{\mathrm{c}} = 70$ mA, $P_{\mathrm{tot}} = 300$ mW, noise figure F_{min} at 350 MHz is less than 1 dB at 5 mA, and the associated gain is more than 17 dB [33].

6 A DESIGN EXAMPLE FOR A 350 MHz FIXED FREQUENCY COLPITTS OSCILLATOR

The following is an exact mathematical solution for designing the 350 MHz Colpitts oscillator.

The circuit consists of the Colpitts configuration following Fig. 1c [33]. In order to have enough loop gain, a microwave transistor BFG520 is used. At the proposed starting DC current of 6 mA (being close to the minimum noise figure current and as a first trial to meet the output power), f_T is 6 GHz. When selecting a transistor with a higher f_T, there is always a possibility of unwanted microwave oscillation and higher flicker noise. When comparing microwave transistors with audio transistors, it becomes apparent that at much lower frequencies, there is much less flicker noise contribution. This transistor can safely be operated at 30 mA but the rule of thumb is when using 10–15% of $I_{c_{max}}$, the flicker contribution is much less. For low-noise operation, the datasheet indicates 1.1 dB spot noise figure at 900 MHz at 5 mA.

The 350 MHz oscillator, using the bipolar transistor BFG520, is designed based on analytical equations and is later verified with simulation results. Based on the output power requirement and harmonics at a given load, the drive level is fixed. The normalized drive level (of $x = 15$) is chosen to allow an adequate drive level to sustain oscillation and, yet, not to produce excessive harmonic content. Figure 6 shows the values of the optimized circuit. While simulating for a series resonant configuration, the value of $C_p = 8.2$ fF was used as a placeholder, based on impedance considerations. C_p was set to 8.2 pF for parallel resonant configuration, the value of $L = 21$ nH, and $C_c = 3.3$ pF was set to achieve oscillation at 350 MHz. Experimenting with the simulation, it turns out that "L_b" set to 0.5 μH gives a much better phase noise, about 10 dB better at 100 Hz offset, but this could not be verified yet in a real circuit.
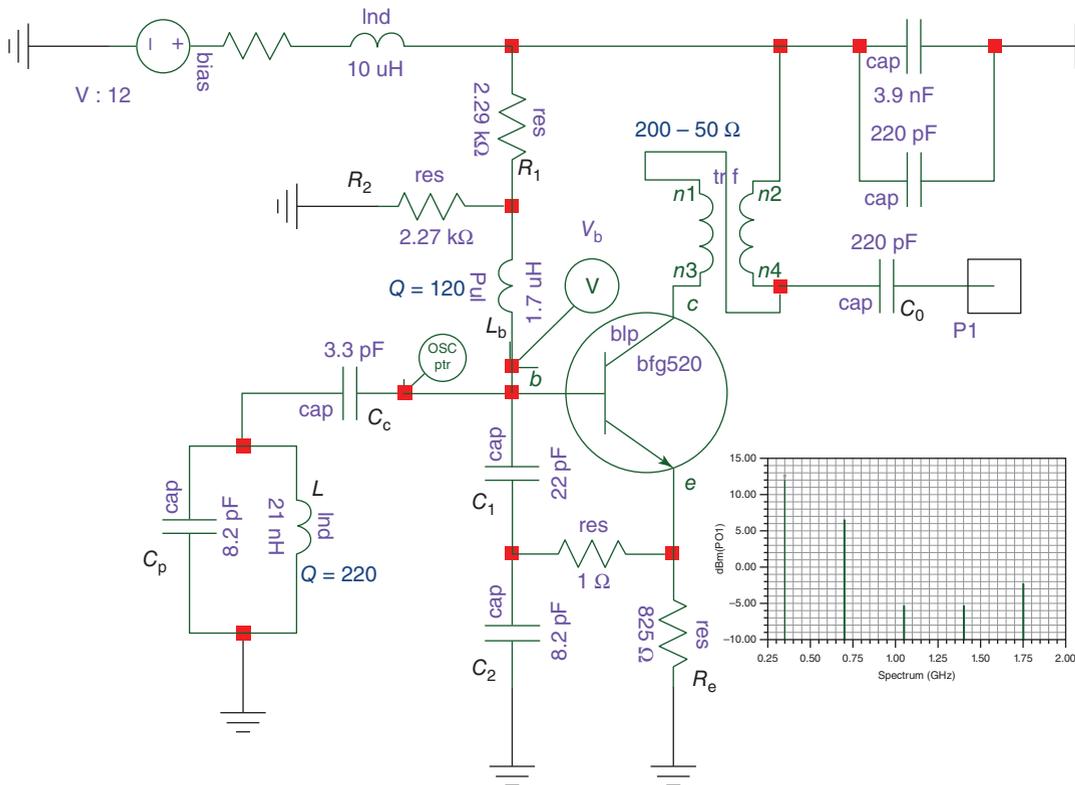
Figure 6 Design of 350 MHz Colpitts oscillator − optimized for phase noise (Rohde and Apte [33]/IEEE).

The output power is taken from the collector and the following is the design procedure. The goal is to obtain an output power over 10 dBm, using a simple design for good understanding.

Step 1:

The normalized drive level will be set at 15, for which the fundamental peak current

$$I_1 \text{ (fundamental)} = 1.932 I_{dc} \text{ (is given from Table 1)}$$

I_1 is the fundamental current specified by the output power needed for the designated load.

The primary impedance of the transformer is 200 Ω and we calculate the RF voltage for $R_L = 200$ Ω and for an output power of $P_{out} \approx 11$ dBm ≈ 14 mW:

$$V_{out} = \sqrt{P_{out} \text{ (mW)} \times 2R_L} = \sqrt{14 \times 10^{-3} \times 2 \times 200} = 2.37 \text{ V}$$

$$\text{(No saturation voltage assumed! This results in slight variation between calculated, simulated,}$$

$$\text{and measured values of P}_{out}.) \tag{41}$$

$$I_1 = \frac{V_{out}}{200} = \frac{2.37}{200} \cong 11.85 \text{ mA} \tag{42}$$

$$I_e = I_{dc} = \frac{I_1}{1.932} = \frac{11.85}{1.932} = 6.13 \text{ mA} \tag{43}$$

Step 2: Biasing

The transistor uses a 12-V power supply and an 825-Ω emitter resistor at ~6 mA, resulting in ~5 V drop, so the transistor can afford a large voltage swing between the base and the ground. This reduces flicker noise (resistive feedback) and distortion. The base voltage divider for reasons pertaining to temperature stability uses a higher-than-normal dc current and is isolated from the base using a RF choke. Frequently, in designs, this circuit trick is not used:

$$V_b = I_e \left[R_e + \frac{R_e}{\beta + 1} \right] + V_{be} = 5.96 \text{ V} \tag{44}$$

β is assumed to be around 100 and V_{be} is approximately 0.8 V. Bias resistors R_1 and R_2 are given as

$$V_b = \frac{R_2}{R_1 + R_2} V_{cc} = 5.96 \text{ V} \Rightarrow \frac{R_1}{R_2} \approx 1 \tag{45}$$

$$R_1 = 2270 \text{ Ω} \tag{46}$$

$$R_2 = 2290 \text{ Ω} \tag{47}$$

$$V_{cc} = 12 \text{ V} \tag{48}$$

The resistor bias current is ~2.6 mA ($V_{cc}/(R_1 + R_2)$).
The base current is 43 μA, so the safety factor is 2.6/0.043 $\cong$ 60.

Step 3: Determination of the large-signal transconductance

Based on Table 2 and $x = 15$, the "DC transconductance" equals

$$Y_{21} = \left. \frac{I_1}{V_1} \right|_{\text{fundamental-freq}} = \frac{1.932 I_{dc}}{1000 \text{ mV}} = \frac{11.85 \text{ mA}}{1000 \text{ mV}} \cong 12 \text{ mS} \tag{49}$$

This is the DC transconductance, meaning the frequency dependence has not been considered.

An analysis of the transistor shows that the small signal transconductance at 6 mA (dc) is about $6 \times 39 \approx 240$ mS. At 350 MHz, this reduces itself to 200 mS down from 240 mS. This is valid only if the transistor does not have any

Table 2 Large-Signal Transconductance as a Function of Drive Level Based on Bessel Function Calculations— $G_m(x)/g_m = 2[I_1(x)/xI_0(x)]$ Versus the Drive Level $= x$

Drive Level: x	$G_m(x)/g_m = 2[I_1(x)/xI_0(x)]$
0.00	1
0.50	0.970
1.00	0.893
2.00	0.698
3.00	0.540
4.00	0.432
5.00	0.357
6.00	0.304
7.00	0.264
8.00	0.233
9.00	0.209
10.00	0.190
15.00	0.129
20.00	0.0975
25.00	0.075

Source: Rohde et al. [5]/John Wiley & Sons.

emitter feedback. In the case of the Colpitts oscillator, we have an emitter resistor which reduces the transconductance; therefore, we have to multiply Y_{21} with

$$\left(\frac{1}{(1/g_m) + R_e} \right) \tag{50}$$

The resulting large-signal loop transconductance Y_{21L} is $\frac{1}{\left(\frac{1}{12\times10^{-3}} + 825\right)} \cong 1.1$ mS, which is an acceptable approximation, as the exact value of x is about 20 (See the simulation results in Fig. 9 for I_c as a function of drive level X) [26, p. 177].

Based on Kirchhoff's law, the following set of equations can be used to determine the feedback factor "n."

$Y_{21L} = 1.1$ mS (DC transconductance—no high-frequency effects included), where $\alpha = 0.99$.

The oscillator circuit with passive component parameters is shown in Fig. 7a.

where

$$Y_1 = G_1 + jB_1 \Rightarrow j\omega C_1, \text{for } G_1 = 0 \tag{51a}$$

$$Y_2 = G_2 + jB_2 \Rightarrow G_2 + j\left[\frac{(\omega^2 LC - 1)\omega C_c}{\omega^2 L(C_c + C) - 1} \right] \tag{51b}$$

G_2 is the loss parameter/load conductance of the resonator connected parallel to the resonator component C_1, C_2 and L, respectively.

$$Y_3 = G_3 + jB_3 \Rightarrow G_3 + j\omega C_2 \tag{51c}$$

G_3 is the conductance of the bias resistor placed across C_2, $1/R_L$ in Fig. 7a.

After doing the proper transformation of the circuit shown in Fig. 7a, we obtain the equivalent circuit as shown in Fig. 7b.
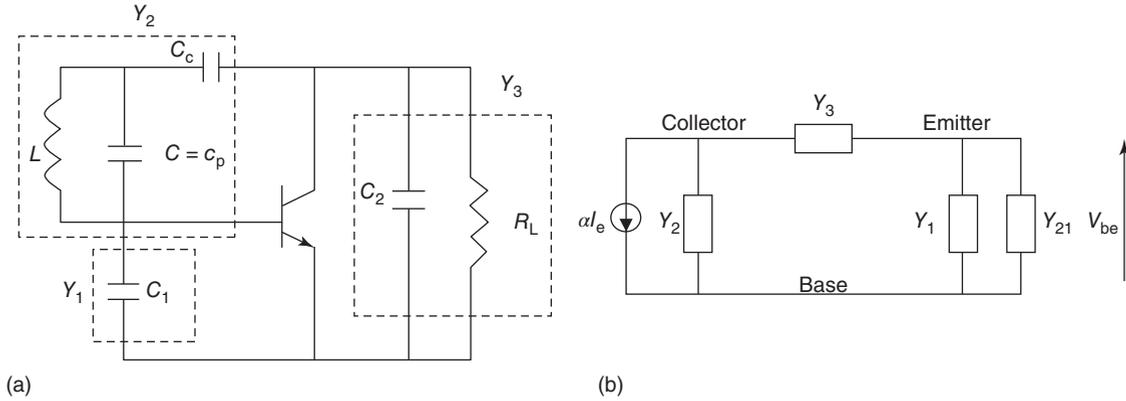
Figure 7 (a) Oscillator circuit with the passive components Y_1, Y_2, and Y_3. (b) Equivalent oscillator circuit for the analysis of the transformed conductance seen by the current source (Rohde et al. [5]/John Wiley & Sons).

The large-signal transconductances Y_{21} and G_1 are transformed to the current source through the voltage divider $\frac{V_{eb}}{V_{cb}}$. The voltage V_{eb} must be added to V_{cb} to calculate the transformation ratio, which is also inverse of the feedback factor and can be written as

$$\frac{V_{eb}}{V_{cb}} = \frac{C_2}{C_1 + C_2} = \frac{1}{n} \tag{51d}$$

And

$$\frac{V_{ce}}{V_{cb}} = \frac{C_1}{C_1 + C_2} = \frac{n-1}{n} \tag{51e}$$

The conductance G_2 is already in parallel with the current source so it remains unchanged. The factor "n" represents the ratio of the collector-base voltage to the emitter-base voltage at the oscillator resonant frequency.

$$G_1 \rightarrow \frac{G_1}{n^2} \tag{51f}$$

$$Y_{21} \rightarrow \frac{Y_{21}}{n^2} \Rightarrow \frac{G_m}{n^2} \tag{51g}$$

$$G_3 \rightarrow \left[\frac{n-1}{n}\right]^2 G_3 \tag{51h}$$

G_2 remains constant.

The transformed conductance is proportional to the square of the voltage ratios given in Eqs. (51d) and (51e), producing a total conductance as seen by the current source at resonance as

$$G_{\text{total}} = G_2 + \frac{G_m + G_1}{n^2} + \left[\frac{n-1}{n}\right]^2 G_3 \tag{51i}$$

For sustained oscillation, the closed-loop gain at resonance is given as

$$\left[\frac{\left(\frac{V_{be}Y_{21}\alpha}{nG_{\text{total}}}\right)}{V_{be}}\right] = 1 \Rightarrow nG_{\text{total}} = Y_{21}\alpha \tag{51j}$$

$$\frac{Y_{21}}{nG_{\text{total}}} = \frac{1}{\alpha} \Rightarrow \frac{Y_{21}}{nG_{\text{total}}} > 1 \tag{51k}$$

α is assumed to be 0.0.99 and variation in the value of α does not influence the expression above greatly. Rearranging the device conductance and circuit conductance, the general oscillator equation, after multiplying (51i) with n on both sides, is written as

$$nG_{\text{total}} = n\left[G_2 + \frac{Y_{21} + G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \tag{51l}$$

$$Y_{21}\alpha = n\left[G_2 + \frac{Y_{21} + G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \Rightarrow \left[\frac{-(1-n\alpha)}{n^2}\right]Y_{21} = \left[G_2 + \frac{G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \tag{51m}$$

$$n^2(G_2 + G_3) - n(2G_3 + Y_{21}\alpha) + (G_1 + G_3 + Y_{21}) = 0 \tag{51n}$$

$$n = \frac{(2G_3 + Y_{21}\alpha) \pm \sqrt{(2G_3 + Y_{21}\alpha)^2 - 4(G_2 + G_3)(G_1 + G_3 + Y_{21})}}{2(G_2 + G_3)} \tag{51o}$$

$$n_1 = \frac{(2G_3 + Y_{21}\alpha)}{2(G_2 + G_3)} + \frac{\sqrt{(2G_3 + Y_{21}\alpha)^2 - 4(G_2 + G_3)(G_1 + G_3 + Y_{21})}}{2(G_2 + G_3)} \tag{51p}$$

$$n_2 = \frac{(2G_3 + Y_{21}\alpha)}{2(G_2 + G_3)} - \frac{\sqrt{(2G_3 + Y_{21}\alpha)^2 - 4(G_2 + G_3)(G_1 + G_3 + Y_{21})}}{2(G_2 + G_3)} \tag{51q}$$

From the quadratic equation above, the value of the factor n can be calculated, and thereby, an estimation of the capacitance can be done a priori.

To ensure higher loop gain, $\boldsymbol{n_1}$ is selected from $n_{\max}[\boldsymbol{n_1,n_2}]$.

Once the value of n is fixed, then the ratio of the capacitance is calculated as

$$\frac{C_2}{C_1 + C_2} = \frac{1}{n} \tag{51r}$$

$$C_2 = \frac{C_1}{n-1} \Rightarrow \frac{C_1}{C_2} = n - 1 \tag{51s}$$

If G_3 and G_1 are zero, then the quadratic equation (51n) reduces to

$$n^2 G_2 - nY_{21}\alpha + Y_{21} = 0 \tag{51t}$$

$$Y_{21} \cong \frac{n^2}{1-n}G_2 \Rightarrow Y_{21} = \left[\frac{n^2}{1-n}\right]\frac{1}{R_p} \tag{51u}$$

$$\frac{Y_{21}R_p}{n} = \frac{n}{1-n} \tag{51v}$$

$$R_P = \frac{1}{G_2}, \quad \frac{Y_{21}R_p}{n} \rightarrow \text{Loop gain} \tag{51w}$$

$$\text{Loop gain}\frac{Y_{21}R_p}{n} \rightarrow 1 \tag{51x}$$

From Eqs. (51r) and (51u)

$$Y_{21} \Rightarrow G_m(x) = \frac{1}{R_p}\frac{[C_1 + C_2]^2}{C_1 C_2} \tag{51y}$$

The quadratic equation for n [from (51n)] is reduced to

$$n^2(G_3) - n(2G_3 + Y_{21}\alpha) + (G_3 + Y_{21}) = 0 \tag{52a}$$

$$G_3 = \frac{1}{R_e} = \frac{1}{825} = 1.21 \text{ mS}$$

$$n^2(1.21) - n(2 \times 1.21 + 1.1 \times 0.99) + (1.21 + 1.1) = 0 \tag{52b}$$

$$1.21n^2 - 3.514n + 2.313 = 0 \tag{52c}$$

$$n = \frac{3.514 \pm \sqrt{(3.514)^2 - 4 \times 1.21 \times 2.313}}{2 \times 1.21} \tag{53}$$

$$n \Rightarrow n_1 = 1.888 \text{ and } n_2 = 1.01 \tag{54}$$

The higher value of the transformation factor, n, is selected as $n = 1.888$.

The ratio for the values of C_1 and C_2 is calculated as

$$\frac{C_2}{C_1 + C_2} = \frac{1}{n} \Rightarrow C_2 = \frac{C_1}{n-1} \tag{55}$$

$$C_2 = \frac{C_1}{n-1} = \frac{C_1}{0.888} \Rightarrow \frac{C_1}{C_2} \cong 0.9 \approx 1 \tag{56}$$

The ratio of the capacitor C_1 to C_2 is 1. For larger transconductance, Y_{21}, $(C_1/C_2) > 1$.

6.1 A Discussion About Drive Level and Noise

The plot in Fig. 8 [5] shows the impact of the normalized drive level "x" on the phase noise. The exact values have to be assessed for individual circuits, but the general trend follows the plot shown.
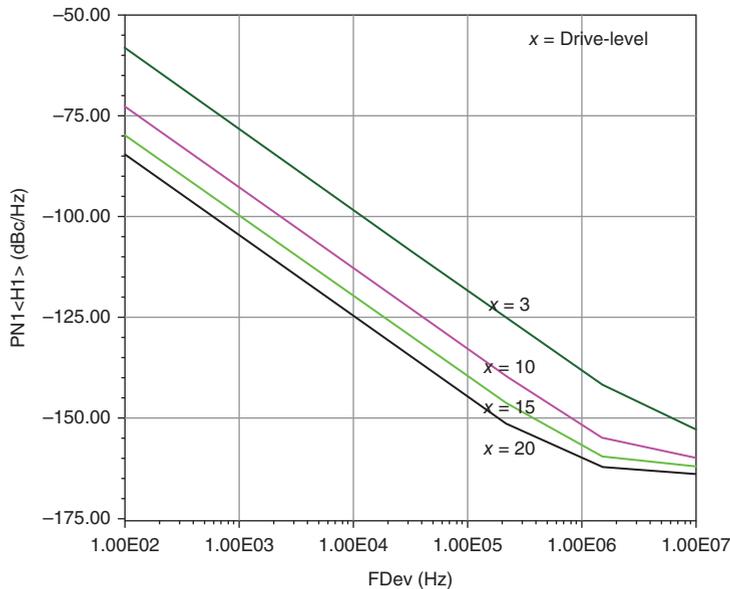
Figure 8 Example for the single sideband phase noise as a function of the normalized drive level x for a high Q 1 GHz oscillator (Rohde et al. [5]/John Wiley & Sons).
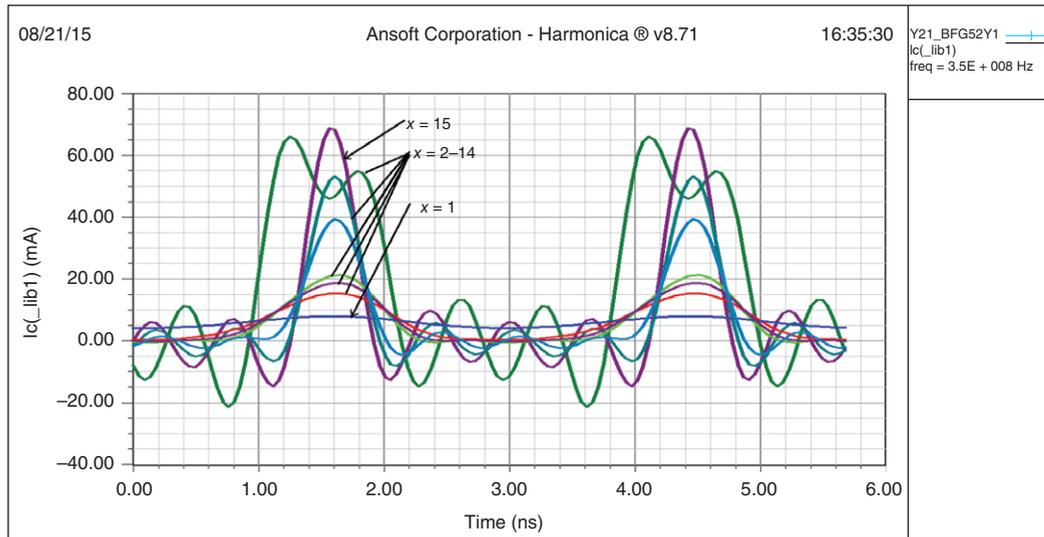
Figure 9 I_c as a function of drive level X [33] is shown (Rohde and Apte [33]/IEEE).

In Fig. 9, $x = 1$ is the linear case (Class A—operation) and the values above $x = 15$ produce narrow pulses. Class A operation gives higher output power but is not optimized for phase noise. However, at higher drive levels, the transistor is "ON" for shorter duration, thus, less loading and better phase noise, but at the cost of lower power output.

If the transistor is overdriven at the base, the collector current folds back (dip) and the actual current gain falls to values of 1.4 in our case (from Fig. 9).

For the uncompressed current gain $(Y_{21}/Y_{11}) \approx (C_2/C_1) \approx 270$ pF/10 pF, the circuit will actually oscillate but does not have acceptable phase noise (low value of x, $n = 28$, where $n = (C_1/C_2) + 1$).

By changing the capacitors C_1/C_2 to 33 pF/10 pF, $n = 4.3$, the phase-noise performance is optimized, as shown in Fig. 10. This circuit is a series-tuned oscillator and now we move on to a high Q (from $Q = 220$ to $Q = 450$)
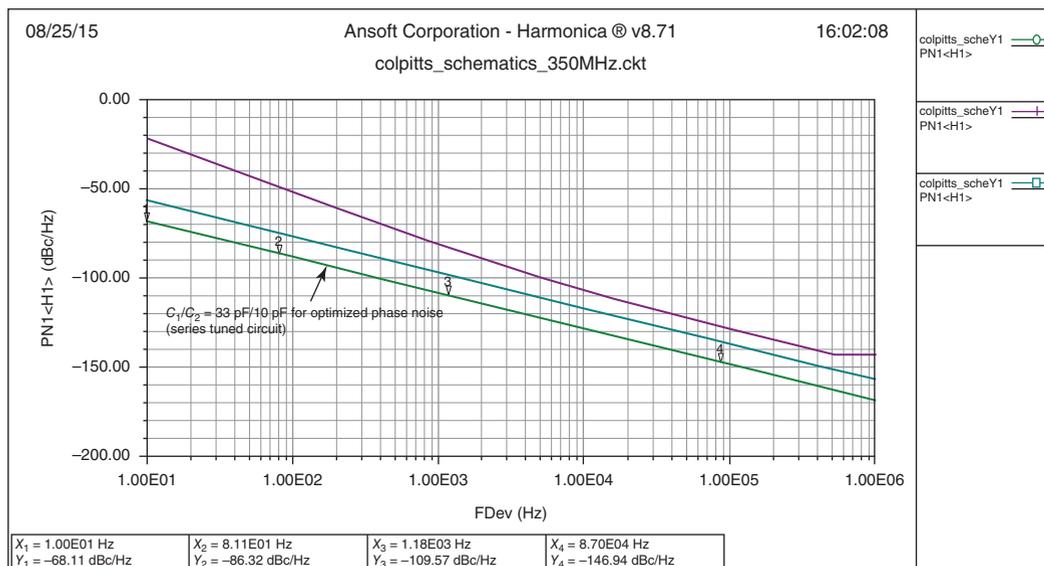
Figure 10 Optimization of phase noise for the series-tuned circuit (Rohde and Apte [33]/IEEE).

circuit, where the resonator is loosely coupled to the transistor. The tuned circuit consists of a 22 nH inductor and an 8.2 pF capacitor. The following shows the design calculation for the parallel-tuned circuit as found in ceramic resonator-based oscillators.

The quality factor of the inductor is assumed 60 at 350 MHz, a low Q case.

The value of inductor is obtained as

$$Q_T = \frac{R_p}{\omega_0 L} \implies L = \frac{3649}{60 \times \omega_0}, \quad \text{where } R_p \text{ is calculated using } G_m(x) = \frac{1}{R_p} \frac{C_1}{C_2} \left[1 + \frac{C_1}{C_2} \right]^2 \tag{57}$$

$$L = \frac{3649}{60 \times 2\pi \times 350 \times E6} \approx 27 \text{ nH} \tag{58}$$

$$\omega = \sqrt{\frac{1}{L} \left[\frac{1}{C_1} + \frac{1}{C_2} \right]} \tag{59}$$

$$\omega^2 = \frac{1}{L} \left[\frac{1}{C_1} + \frac{1}{C_2} \right] = \frac{C_1 + C_2}{L C_1 C_2} \tag{60}$$

The value of the capacitor is determined as

$$C_2 = \frac{2.55}{\omega^2 \times 17\text{E} - 9} \approx 14 \text{ pF} \tag{61}$$

$$C_1 \approx C_2 \approx 14 \text{ pF} \tag{62}$$

Taking into consideration the actual parasitics and RF parameters of the transistor, the optimized values are $C_1 = 12$ pF and $C_2 = 8.2$ pF.

Step 4: Calculation of the coupling capacitor C_c: [5, Eq. (C.23)]

The expression for the coupling capacitor is

$$\frac{C}{10} > C_c > \left\{ \frac{(\omega^2 C_1 C_2) \left(1 + \omega^2 Y_{21}^2 L_P^2 \right)}{\left[\left(Y_{21}^2 C_2 - \omega^2 C_1 C_2 \right) \left(1 + \omega^2 Y_{21}^2 L_P^2 \right) (C_1 + C_P + C_2) \right]} \right\} \tag{63}$$

$$C_c = 3.3 \text{ pF} \tag{64}$$

Step 5: Calculation of the phase noise of the Colpitts oscillator:

The mathematical expression of the phase noise of a Colpitts oscillator is [5, p. 180]:

$$L(\omega) = 10 \log \left\{ \left[\left[4kTR + \left[\frac{4qI_c g_m^2 + \frac{K_f I_b^{AF}}{\omega} g_m^2}{\omega_0^2 C_1^2 \left(\omega_0^2 (\beta^+)^2 C_2^2 + g_m^2 \frac{C_2^2}{C_1^2} \right)} \right] \right] \left[\frac{\omega_0^2}{4\omega^2 V_{cc}^2} \right] \left[\frac{1}{Q^2} + \frac{[C_1 + C_2]^2}{C_1^2 C_2^2 \omega_0^4 L^2} \right] \right\} \tag{65}$$

where

$$\beta^+ = \left[\frac{Y_{21}^+}{Y_{11}^+} \right] \left[\frac{C_1}{C_2} \right]^p \quad g_m = \left[Y_{21}^+ \right] \left[\frac{C_1}{C_2} \right]^q$$

where values of p and q depend on the drive level (x).

Y_{21}^+, Y_{11}^+ is the large-signal $[Y]$ parameter of the active device;

K_f is the flicker noise coefficient;

AF is the flicker noise exponent;

$\text{£}(\omega)$ is the ratio of sideband power in a 1 Hz BW at ω to total power in dB;

ω is the frequency offset from the carrier;

ω_0 is the center frequency;

Q_L is the loaded Q of the tuned circuit;

Q_O is the unloaded Q of the tuned circuit;

kT is the 4.1×10^{-21} at 300 K (room temperature);

R is the equivalent loss resistance of the tuned resonator circuit;

I_c is the RF collector current;

I_b is the RF base current;

V_{cc} is the RF collector voltage;

C_1, C_2 is the feedback capacitor.

Using a Mathcad calculation, we obtain the following results as shown in Fig. 11 [5, Eq. 8.109], which compares well with the measured data.

Phase noise equation

$I_c := 6.2 \cdot 10^{-3}$ $I_b := 43.2 \cdot 10^{-6}$ $L := 22 \cdot 10^{-9}$ $C_1 := 12 \cdot 10^{-12}$ $C_2 := 8.2 \cdot 10^{-12}$ $C_c := 3.3 \cdot 10^{-12}$

$K := 1.3806 \cdot 10^{-23}$ $T := 300$ $KT := 4.143 \cdot 10^{-21}$ $R := 0.3$ $K_f := 1 \cdot 10^{-7}$ $AF := 2$

$Q := 60$ $V_{CC} := 12$ $f := 350 \cdot 10^6$ $w_0 := 2\,\pi \cdot f$ $\beta := 140$

$r_e := \dfrac{26 \cdot 10^{-3}}{Ic}$ $gml := \dfrac{1}{r_e}$ $gml := 0.238$ $q := 1.602 \cdot 10^{-19}$ $i := 0 \ .. \ 7$ $f_{oi} := 10^i$

w_{oi} is the frequency offset from the carrier $w_{oi} := 2 \cdot \pi \cdot f_{oi}$

$$Lw_i := 10 \cdot \log \left[\left[\left[4 \cdot KT \cdot R + \frac{4 \cdot q \cdot Ic \cdot gml^2 + \dfrac{Kf \cdot Ib^{AF}}{w_{oi}} \cdot gml^2}{(w_0)^2 \cdot C_1{}^2 \cdot \left[(w_0)^2 \cdot \beta^2 \cdot C_2{}^2 + gml^2 \cdot \dfrac{C_2{}^2}{C_1{}^2} \right]} \right] \right] \left[\frac{w_0{}^2}{4 \cdot (w_{oi})^2 \cdot V_{cc}{}^2} \left[\frac{1}{Q^2} + \frac{(C_1 + C_2)^2}{C_1{}^2 \cdot C_2{}^2 \cdot (w_0)^4 \cdot L^2} \right] \right] \right]$$

f_{oi}	L_{wi}
1	−5.227
10	−35.222
100	−65.165
$1 \cdot 10^3$	−94.633
$1 \cdot 10^4$	−121.303
$1 \cdot 10^5$	−143.272
$1 \cdot 10^6$	−163.529
$1 \cdot 10^7$	−183.555

Figure 11 Mathcad calculation for phase noise (Rohde and Apte [33]/IEEE).

R & S FSUP 8 Signal Source Analyzer					Locked
Settings		**Residual noise [T1 w/o spurs]**		**Phase Detector + 20 dB**	
Signal frequency:	350.000030 MHz	Int PHN (1.0 .. 10.0 M)	−2.7 dBc		
Signal level:	10.67 dBm	Residual PM	59.306 °		
Cross corr mode:	Harmonic 1	Residual FM	1.106 kHz		
Internal ref tuned	Internal Phase Det	RMS jitter	470.6825 ps		

Phase noise [dBc/Hz]
RF atten   5 dB
Top 10 dBc/Hz

Spot noise   [T1 w/o spurs]
100.000 Hz   −65.31 dBc/Hz
1.000 kHz   −97.40 dBc/Hz
10.000 kHz   −129.32 dBc/Hz
100.000 kHz   −144.37 dBc/Hz
502.929 kHz   −146.28 dBc/Hz

1 CLRWR
SMTH 3%
2 CLRWR

LoopBW

SPR OFF
TH 0dB

A

Figure 12   Measured phase-noise result for 350 MHz oscillator (Rohde and Apte [33]/IEEE).

7   MEASURED RESULTS FOR A 350 MHz OSCILLATOR

The measured phase noise of the oscillator shown in Fig. 12 is not quite comparable with the mathematics because it has a two-stage buffer amplifier which isolates the oscillator from the output termination. This explains the limit of −146 dBc/Hz at far offset. At close-in, the phase noise is influenced by an AFC circuit. The real comparison should be done between 10 Hz and 10 kHz offsets.

In order to optimize the phase noise for this type of oscillator, using discrete components, the selection of the following set of values: $C_p = 8.2$ pF, $L = 21$ nH, $C_1 = 22$ pF, $C_2 = 8.2$ pF, $C_c = 3.3$ pF improved the phase noise from −122 to −125 dBc/Hz at 10 kHz offset. This is a result of trial-and-error, as we do not know all the parasitics. Figure 13a shows the simulated phase-noise plot and Fig. 13b shows further improvement after optimizing the circuit for phase noise.

If we replace the parallel-tuned circuit with a ceramic resonator (at this frequency range, ε_r will be 88, the L/C ratio will be 0.048 nH/pF versus 2.44 nH/pF in the case of discrete components used in our case), and the simulated phase noise is 105 dBc/Hz at 10 kHz offset.

Note: *This is due to the fact that the characteristic impedance of a ceramic resonator is much lower than the discrete case*. $Z_0 = 60\,\Omega\,\dfrac{1}{\sqrt{\varepsilon_r}}\ln\dfrac{D}{d}$ (where D is the outer diameter and d is the inner diameter of the ceramic resonator [12, p. 754]. The prediction agrees well with the measured phase noise [12, Fig. 5.37].
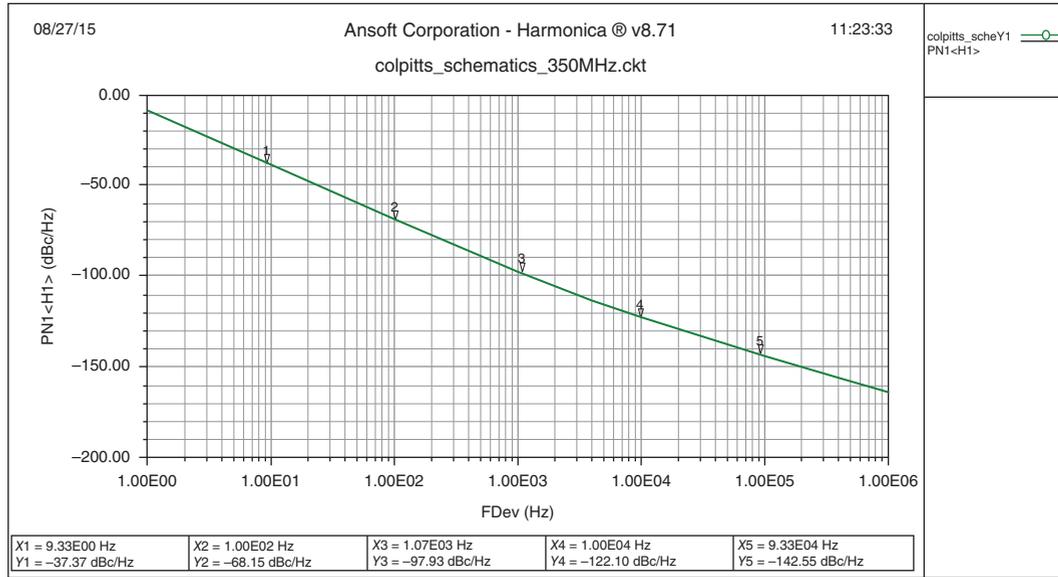
(a)
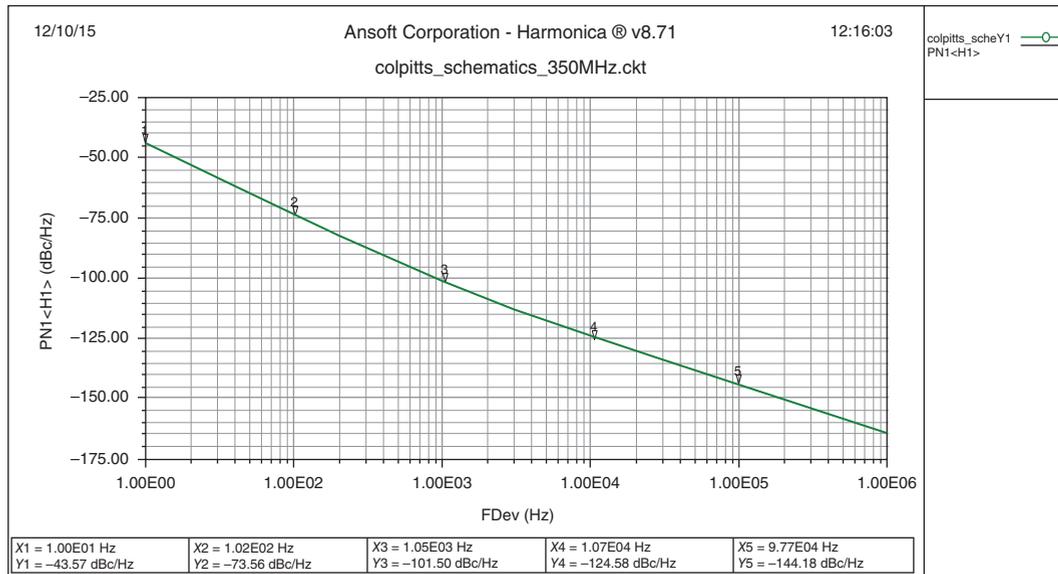
(b)

Figure 13 (a) Simulated phase noise for the 350 MHz parallel tuned Colpitts configuration. (b) Optimized–simulated phase noise for the 350 MHz parallel tuned Colpitts configuration (Rohde and Apte [33]/IEEE).

Figure 14 shows the plots of the collector and base currents I_c and I_b for the optimized case ($C_p = 8.2$ pF, $L = 21$ nH ($Q = 60$ at 350 MHz), $C_c = 3.3$ pF, $C_1 = 12$ pF, $C_2 = 8.2$ pF).

From the plot in Fig. 14, we can determine that the ratio of large-signal $(Y_{21}/Y_{11}) = \beta = 1.4$. The next important parameter, shown in Fig. 15, is for the normalized drive level (x) is $V_1/(kT/q)$.

From Fig. 15, the root mean square (RMS) value of V_{be} is used to determine the approximate drive level. Since

$$V_{be} = V_1, \text{ drive level } (x) \approx \frac{500 \text{ mV}_{\text{rms}}}{26 \text{ mV}} \approx 20 \tag{66}$$
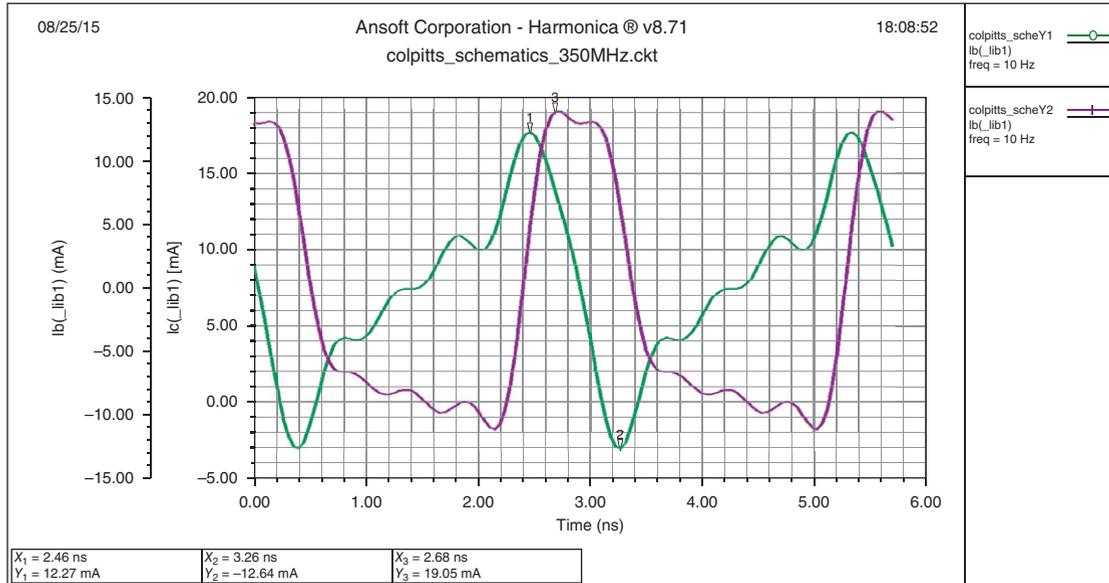
Figure 14 Y_{21}/Y_{11} large-signal condition (Rohde and Apte [33]/IEEE).
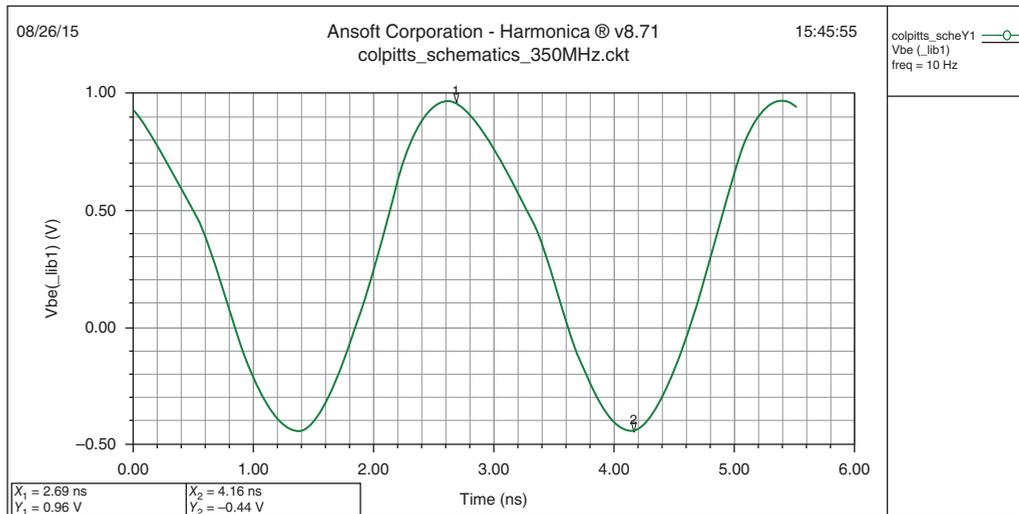
Figure 15 V_{be}—to calculate the drive level (Rohde and Apte [33]/IEEE).

A table of normalized transconductance as a function of the drive level including the large values is given in Table 2 [5].

Figures 16 and 17a show the phase-noise variation with variation in Q ($L = 22$ nH) in the LC resonator. The output power, collector current, and base voltage (V_b) and (V_{be}) plots are also shown for the same combination.

The parallel-tuned circuit shows better phase-noise performance, as seen in Fig. 17b, due to the fact that the rate of change of reactance in a parallel-tuned circuit is significantly larger than that in a simple series-tuned oscillator.

After evaluating and optimizing several design parameters, a sanity check for the assumptions made is the last step. What is needed is a time-domain simulation to verify that no saturation occurs. Using LTSpice, the plot as shown in Fig. 18 is obtained.
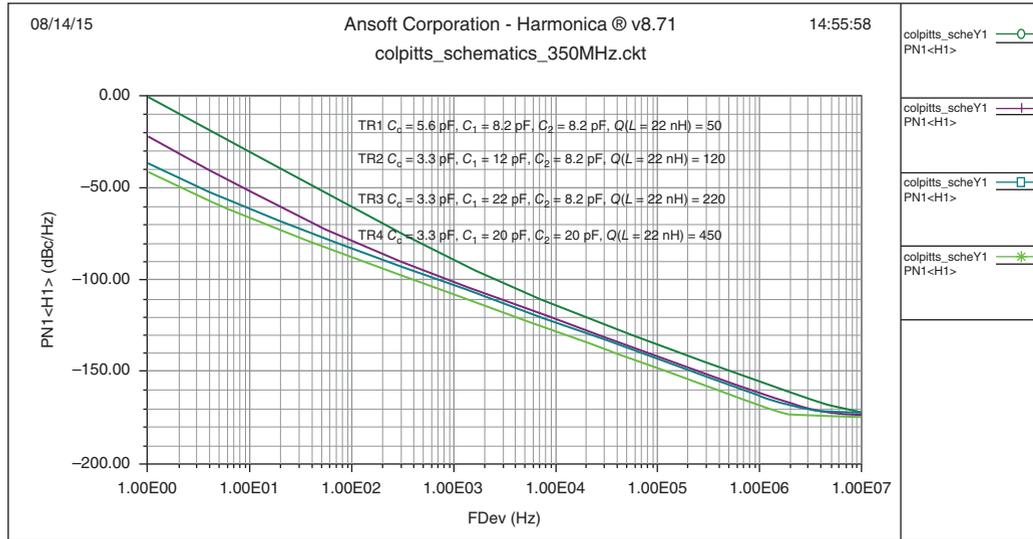
Figure 16 Optimized phase noise for different values of inductor Q (Rohde and Apte [33]/IEEE).

In Fig. 18, the green line records the collector/emitter voltage. It clearly drops to only small fractions of a volt, indicating a deep saturation over almost all the time where the transistor draws current. The collector current (cyan curve) only has a remote similarity to the harmonic balance results. BE voltage (red) is comfortably below the breakdown value (2.5 V). Harmonic contents are much larger than the harmonic balance (HB) predictions (possible due to an insufficiently small number of harmonics in the HB run).

The observations above show that:

1. It is risky to rely on a too small set of transistor physics to make derivations or optimize a circuit: large-signal circuits often deviate grossly from small signal approximations.
2. If assumptions are made, they must be verified a posteriori if they hold or not (e.g., no saturation).
3. Phase-noise curves are no proof that the underlying physics is correctly modeled. A match between theory and experiment can almost always be accomplished by tuning the many magic screws of Leeson's formula (Q_L, Af, KF, K…).
4. Obviously, saturation is no killer criterion for low-noise performance. The performance of the present circuit is good even with deep saturation present.
5. Some of the insights gained from the linearized models still hold (e.g., the recommendation to keep conduction angles low or that noise is improved by a large C_1/C_2 ratio), but the predicted optimum values are not correct. Full-physics simulations can bridge the gap here and allow a successful fine-tuning with a valid physical model in the background not using questionable simplifications.

A better understanding of oscillators in detail is the focus of ongoing research work to come.

7.1 Validation Circuits

The following section is based on Ref. 5, chaps. 7–10.

Chapter 7 of Ref. 5 developed the mathematical background for optimizing microwave oscillators. The next step is to validate the synthesis of the circuits. The following circuits have been chosen for validation:

- 100 MHz crystal oscillator.
- 1000 MHz bipolar transistor-based oscillator with ceramic resonator.
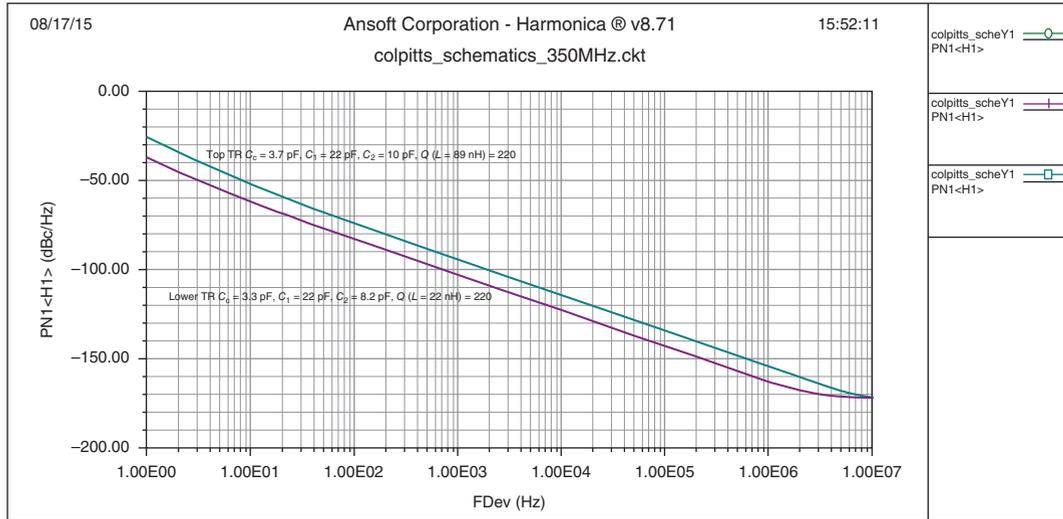
(a)
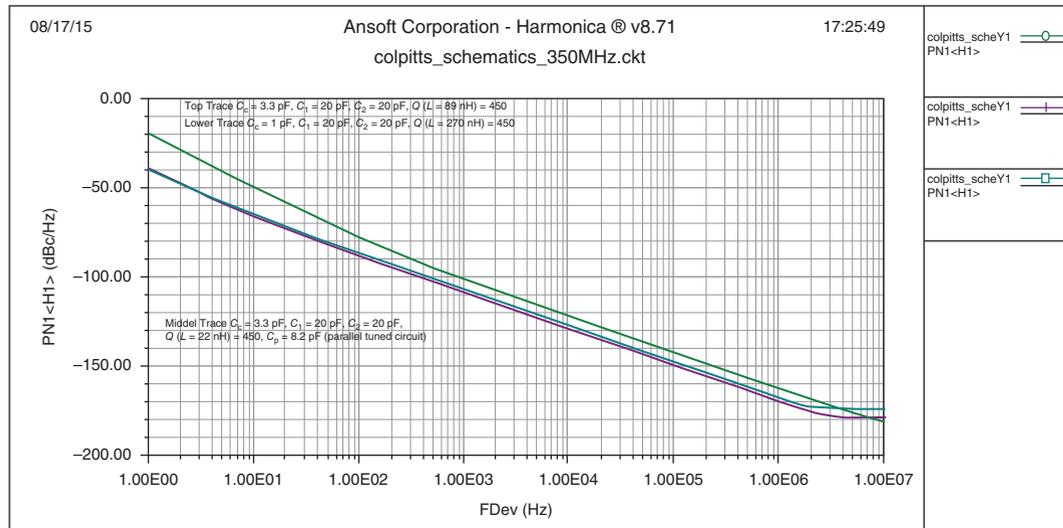
(b)

Figure 17 (a) Results of series and parallel-tuned circuits for the same value of inductor Q. (b) Results of series- and parallel-tuned circuits for higher value of inductor Q (Rohde and Apte [33]/IEEE).

- 4100 MHz bipolar transistor-based oscillator with transmission line resonators.
- 2000 MHz GaAs FET-based oscillator with transmission line resonators.

7.2 100 MHz Crystal Oscillator (XO)

For many synthesizers, a 100 MHz frequency standard is required. Here is a design example based on the phase-noise analysis of the feedback model.

Up to here, we have calculated both the large-signal drive condition and the optimum choice of the feedback capacitance. Now, we are going to consider the oscillator as a feedback loop with a noisy transistor, looking at
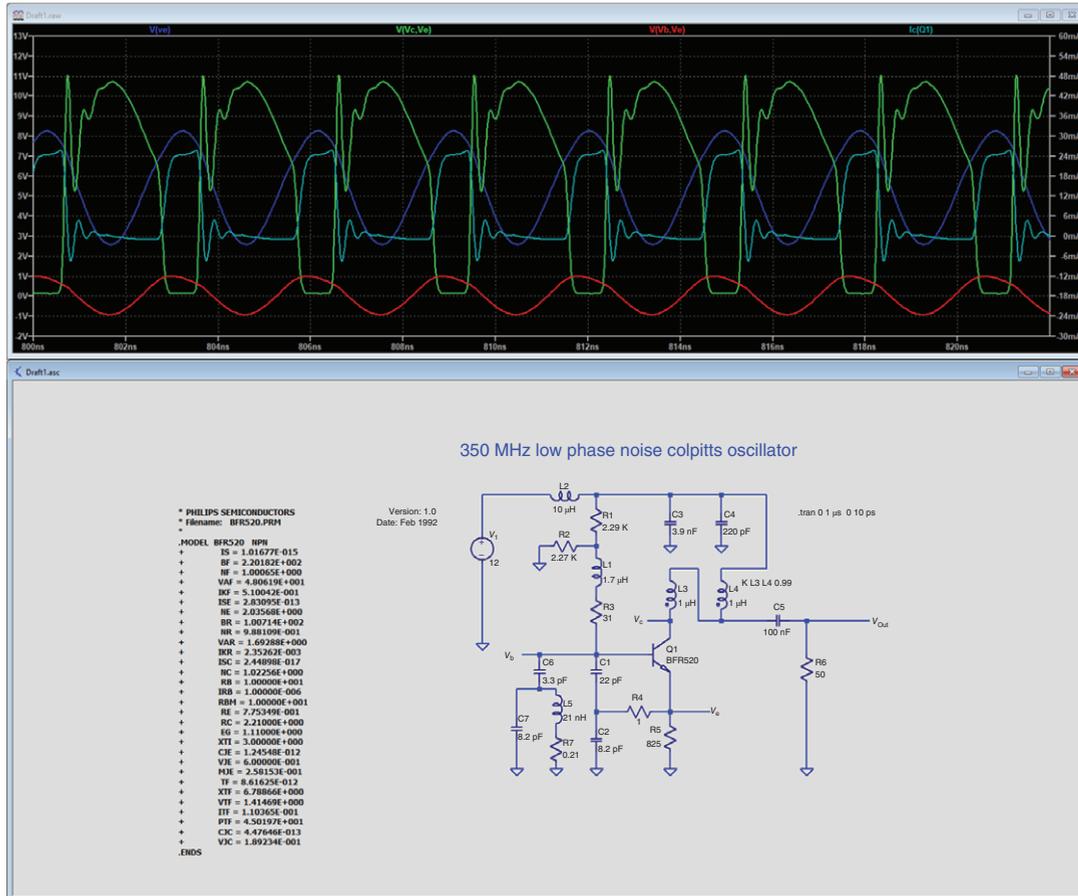
Figure 18 Time-domain simulation to verify that no saturation occurs using LTSpice.
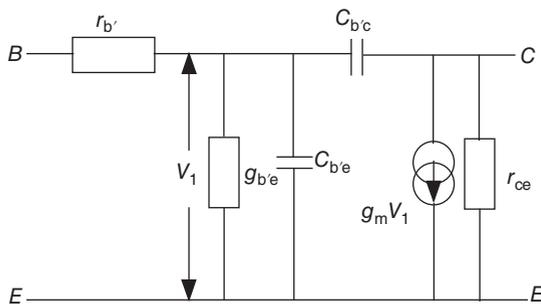
Figure 19 Grounded emitter bipolar transistor (Rohde et al. [5]/John Wiley & Sons).

all typical noise contributions. Based on a fixed set of values of C_1 and C_2, we can now calculate the accurate phase-noise behavior of the oscillator and analyze the various noise contributions.

First, the noisy bipolar transistor will be introduced. Figure 19 shows the familiar hybrid-π transistor circuit and Fig. 20 shows the equivalent circuit with the relevant noise sources included.
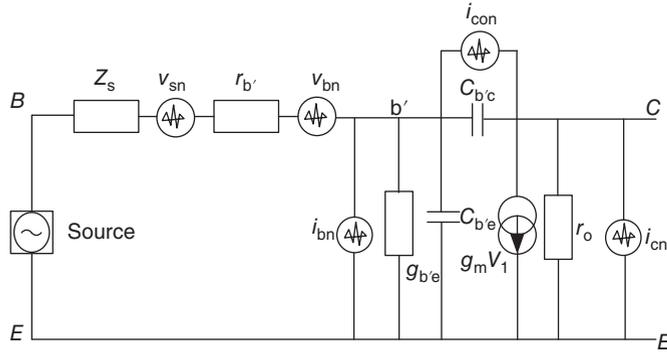
Figure 20 Hybrid-π configuration of the grounded bipolar transistor with noise sources (Rohde et al. [5]/John Wiley & Sons).

The mean square value of the noise generators in Fig. 20, in a narrow frequency offset Δf, is given by

$$\overline{i_{bn}^2} = 2qI_b\Delta f \tag{67}$$

$$\overline{i_{cn}^2} = 2qI_c\Delta f \tag{68}$$

$$\overline{i_{con}^2} = 2qI_{cob}\Delta f \tag{69}$$

$$\overline{v_{bn}^2} = 4kTR_b\Delta f \tag{70}$$

$$\overline{v_{sn}^2} = 4kTR_S\Delta f \tag{71}$$

where I_b, I_c, and I_{cob} are average DC currents over the Δf noise bandwidth.

The noise power spectral densities due to these noise sources are

$$S(i_{cn}) = \frac{\overline{i_{cn}^2}}{\Delta f} = 2qI_c = 2KTg_m \tag{72}$$

$$S(i_{bn}) = \frac{\overline{i_{bn}^2}}{\Delta f} = 2qI_b = \frac{2KTg_m}{\beta} \tag{73}$$

$$S(i_{fn}) = \frac{K_f I_b^{AF}}{f} \tag{74}$$

$$S(v_{bn}) = \frac{\overline{v_{bn}^2}}{\Delta f} = 4KTr_b' \tag{75}$$

$$S(v_{sn}) = \frac{\overline{v_{sn}^2}}{\Delta f} = 4KTR_s \tag{76}$$

where r_b' and R_s are base and source resistance and Z_s is the complex source impedance.

Figure 21a shows the feedback arrangement for the Colpitts oscillator with the noise sources.

If we include saturation in our model, the Schottky noise formula for the collector current is no longer valid. Schottky noise emerges when carriers cross a potential gap [like the common base (CB) space charge zone]. If the tone disappears due to flooding, then noise levels fall drastically and subside on the level of a small resistance noise. So, the S(icn) term **overestimates** the collector noise in case of saturation.

2-Port representation of bipolar transistor
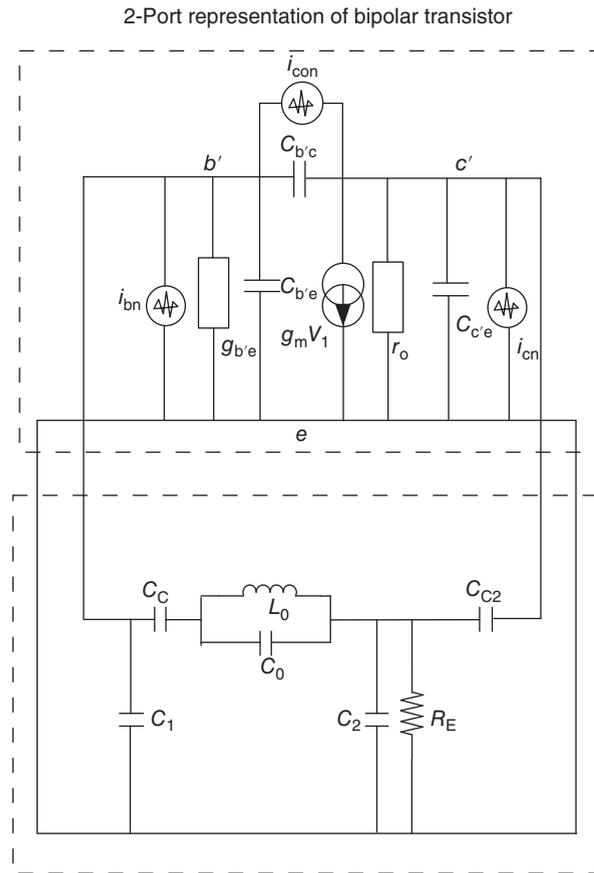
(a)   2-port representation of feedback-network
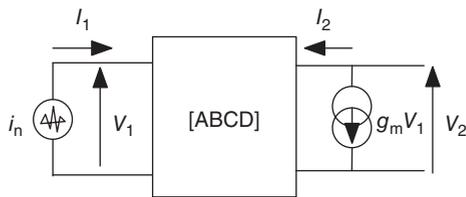
(b)   Feedback-network

Figure 21   (a) Feedback arrangement for the Colpitts oscillator with the noise sources. (b) Linear representation of feedback Colpitts oscillator with input white noise source $i_n(\omega)$ (Rohde et al. [5]/John Wiley & Sons).

The transistor is acting like a gain block. The feedback network includes the load conductance and a small part of the output signal goes to the input of the bipolar transistor through the resonant circuit. The *ABCD* chain matrix will be used for the analysis.

This is not consistent with Fig. 21a, but useful because all non-active components are now in the feedback network.

The input noise power spectral density can be given as

$$S_{\text{in}} = \frac{\left| \overline{i_n^2} \right|}{\Delta f} \tag{77}$$

where

$$\left| \overline{i_n^2} \right| = \sum_{i=1}^{i=N} \left| \overline{i_{ni}^2} \right| = \left| \overline{i_{n1}^2} \right| + \left| \overline{i_{n2}^2} \right| + \left| \overline{i_{n3}^2} \right| \dots \dots \dots + 2C_{ii} \left[i_{ni} i_{n(i+1)}^{\bullet} \right] \tag{78}$$

and C_{ii} is the noise correlation coefficient.

Figure 21b shows the linear representation of the Colpitts oscillator with the input white noise source $i_n(\omega)$.

The [$ABCD$] matrix of above oscillator circuit can be given as

$$[A] = 1 + \left[\left(\frac{1}{j\omega C_c} + \frac{j\omega L_0}{1 - \omega^2 L_0 C_0} \right) \left(j\omega C_2 + \frac{1}{R_E} \right) \right]$$

$$[B] = \frac{1}{j\omega C C_2} + \left(\frac{1}{j\omega C_c} + \frac{j\omega L_0}{1 - \omega^2 L_0 C_0} \right) \left[1 + \left(j\omega C_2 + \frac{1}{R_E} \right) \left(\frac{1}{j\omega C C_2} \right) \right]$$

$$[C] = j\omega C_1 + \left(j\omega C_2 + \frac{1}{R_E} \right) \left[1 + j\omega C_1 \left(\frac{1}{j\omega C_c} + \frac{j\omega L_0}{1 - \omega^2 L_0 C_0} \right) \right]$$

$$[D] = \frac{C_1}{C C_2} + \left[\left[1 + j\omega C_1 \left(\frac{1}{j\omega C_c} + \frac{j\omega L_0}{1 - \omega^2 L_0 C_0} \right) \right] \left[1 + \left(j\omega C_2 + \frac{1}{R_E} \right) \left(\frac{1}{j\omega C C_2} \right) \right] \right] \tag{79}$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{80}$$

$$V_1 = AV_2 - BI_2 \tag{81}$$

$$I_1 = CV_2 - DI_2 \tag{82}$$

$$Z_{\text{in}} = \left[\frac{V_1}{I_1} \right]_{I_2=0} = \frac{A}{C} \tag{83}$$

where

$$I_1 = i_n \tag{84}$$

$$I_2 = -g_m V_1 \tag{85}$$

The equivalent input noise voltage due to the input noise current, $I_1 = i_n$, is

$$v_n(\omega) = I_1 Z_{\text{in}} = I_1 \left[\frac{V_1}{I_1} \right]_{I_2=0} = I_1 \left[\frac{A(\omega)}{C(\omega)} \right] = i_n \left[\frac{A(\omega)}{C(\omega)} \right] \tag{86}$$

The input noise voltage $v_n(\omega)$ will produce two narrowband (1 Hz) uncorrelated components in the frequency domain located at $\omega - \omega_0$ and $\omega + \omega_0$ as $[v_n(\omega)]_{\omega=\omega_0-\Delta\omega}$ and $[v_n(\omega)]_{\omega=\omega_0+\Delta\omega}$.

In the presence of the two uncorrelated components of the input noise voltage, $[v_n(\omega)]_{\omega=\omega_0-\Delta\omega}$ and $[v_n(\omega)]_{\omega=\omega_0+\Delta\omega}$, the peak carrier signal of amplitude V_c at frequency $\omega = \omega_0$ is modulated with an input phase-noise signal $S_{\Delta\phi_{\text{in}}}(\omega)$.

The input phase-noise spectral density at an offset of $\Delta\omega$ is

$$S_{\Delta\phi_{\text{in}}}(\Delta\omega) = \frac{\left| [v_n(\omega)]^2_{\omega=\omega_0-\Delta\omega} \right| + \left| [v_n(\omega)]^2_{\omega=\omega_0+\Delta\omega} \right|}{\left| V_c^2(\omega) \right|} \tag{87}$$

$$S_{\Delta\phi_{\text{in}}}(\Delta\omega) = \frac{2\left|\overline{[v_n(\omega)]^2}\right|}{\left|\overline{V_c^2(\omega)}\right|} \tag{88}$$

$$S_{\Delta\phi_{\text{in}}}(\Delta\omega) = \frac{2\left|\overline{[v_n(\omega)]^2}\right|}{\left|\overline{V_c^2(\omega)}\right|} = 2\frac{\left|\overline{[i_n(\omega)]^2}\right|\left|\overline{A^2(\omega)}\right|}{\left|\overline{V_c^2(\omega)}\right|\left|\overline{C^2(\omega)}\right|} \tag{89}$$

$$\left|\overline{i_n^2}\right| = S_{\text{in}}\Delta f \tag{90}$$

$$\left|\overline{i_n^2}\right|_{\Delta f=1\text{ Hz}} = S_{\text{in}} \tag{91}$$

$$S_{\Delta\phi_{\text{in}}}(\Delta\omega) = 2\frac{S_{\text{in}}\left|\overline{A^2(\omega)}\right|}{\left|\overline{V_c^2(\omega)}\right|\left|\overline{C^2(\omega)}\right|} \tag{92}$$

where S_{in} and $S_{\Delta\phi_{\text{in}}}$ are the input noise power and phase-noise spectral density, respectively.

Based on Refs. 5, chap. 8, 35, 36

$$S_{\Delta\phi_{\text{out}}}(\omega) = S_{\Delta\phi_{\text{in}}}(\omega)\left[1 + \frac{1}{\omega^2}\left(\frac{\omega_0}{2Q_L}\right)^2\right] \tag{93}$$

$$Q_L(\omega = \omega_0) = \frac{\omega_0}{2}\left|\frac{d\phi}{d\omega}\right|_{\omega=\omega_0} \tag{94}$$

The open loop gain is

$$G_{\text{open}}(\omega = \omega_0) = -\left[\frac{g_m}{C(\omega_0)}\right] \tag{95}$$

For sustained oscillation,

$$G_{\text{open}}(\omega = \omega_0) = 1. -\left[\frac{g_m}{C(\omega_0)}\right] = 1 \Rightarrow C(\omega)_{\omega=\omega_0} \text{ is real and negative}$$

$$C(\omega_0) = C_{\text{Real}}(\omega_0) + jC_{\text{Imag}}(\omega_0) \tag{96}$$

$$C_{\text{Imag}}(\omega_0) = 0 \tag{97}$$

$$C_{\text{Real}}(\omega_0) = -g_m \tag{98}$$

$$\left[\frac{d\phi}{d\omega}\right]_{\omega=\omega_0} \approx -\frac{1}{C_{\text{Real}}(\omega_0)}\left[\frac{dC_{\text{Imag}}(\omega)}{d\omega}\right]_{\omega=\omega_0} \tag{99}$$

$$Q_L(\omega = \omega_0) = \frac{\omega_0}{2}\left|\frac{d\phi}{d\omega}\right|_{\omega=\omega_0} \tag{100}$$

$$Q_L(\omega = \omega_0) = \frac{\omega_0}{2} \left| \frac{1}{C_{\text{Real}}(\omega_0)} \left[\frac{dC_{\text{Imag}}(\omega)}{d\omega} \right] \right|_{\omega=\omega_0} \tag{101}$$

$$S_{\Delta\phi_{\text{out}}}(\Delta\omega) = S_{\Delta\phi_{\text{in}}}(\Delta\omega) \left[1 + \frac{1}{(\Delta\omega^2)} \left[\frac{C_{\text{Real}}(\omega_0)}{\left(\frac{dC_{\text{Imag}}(\omega)}{d\omega} \right)} \right]_{\omega=\omega_0}^2 \right] \tag{102}$$

$$S_{\Delta\phi_{\text{in}}}(\Delta\omega) = 2 \frac{S_{\text{in}} \left| \overline{A^2(\omega)} \right|}{\left| \overline{V_c^2(\omega)} \right| \left| \overline{C^2(\omega)} \right|} \tag{103}$$

$$S_{\Delta\phi_{\text{out}}}(\Delta\omega) = 2 \frac{S_{\text{in}}}{\left| \overline{V_c^2(\omega_0)} \right|} \frac{\left| \overline{A^2(\omega_0)} \right|}{\left| \overline{C^2(\omega_0)} \right|} \left[1 + \frac{1}{(\Delta\omega^2)} \left[\frac{C_{\text{Real}}(\omega_0)}{\left(\frac{dC_{\text{Imag}}(\omega)}{d\omega} \right)} \right]_{\omega=\omega_0}^2 \right] \tag{104}$$

We now perform the noise analysis of the Colpitts oscillator.

7.3   Individual Contribution of all Four Noise Sources

The following contribute to the noise of the oscillator:

- thermal noise associated with the loss resistance of the resonator,
- thermal noise associated with the base resistance of the transistor,
- shot noise associated with the base bias current, and
- shot noise associated with the collector bias current.

If we now use the oscillator circuit with a noisy resonator, we can calculate the total noise of the oscillator as shown in Fig. 22.

7.4   Noise Shaping Function of the Resonator

For phase-noise analysis, the oscillator is considered as a feedback system and a noise source is present in the input as shown in Fig. 23.
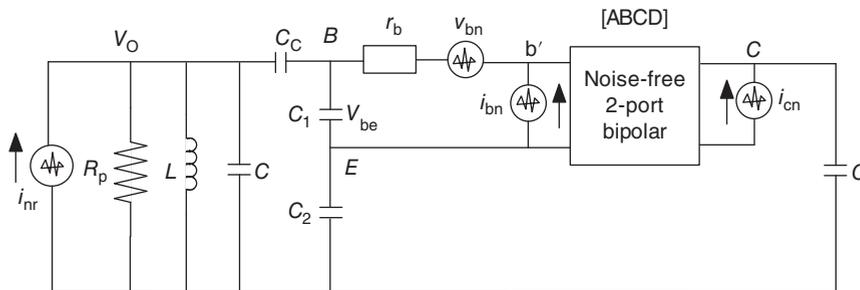
Figure 22   The oscillator circuit with 2-port [*ABCD*] matrix, consistent with the approach of Figs. 8–18 (Rohde et al. [5]/John Wiley & Sons).
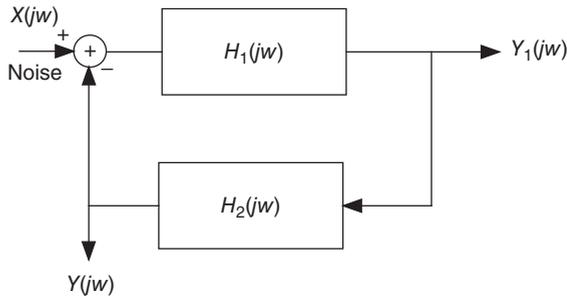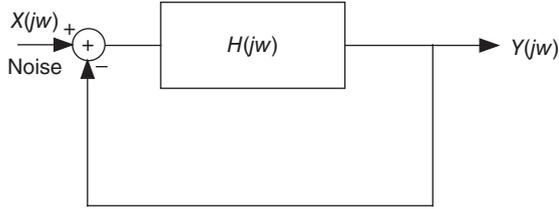
Figure 23 Feedback oscillator with noise source (Rohde et al. [5]/John Wiley & Sons).

Oscillator output phase noise is a function of

- the amount of the source noise present at the input of the oscillator circuit, and
- how much the feedback system rejects or amplifies various noise components.

The unity-gain system closed-loop transfer function is

$$[\text{TF}(j\omega)]_{\text{closed-loop}} = \frac{Y(j\omega)}{X(j\omega)} = \frac{H(j\omega)}{1 + H(j\omega)} \tag{105}$$

$$[H(j\omega)]_{\omega=\omega_0} = -1 \tag{106}$$

For frequencies close to $\omega = \Delta\omega + \omega_0$, the open loop transfer function is

$$[H(j\omega)]_{\omega=\omega_0+\Delta\omega} \approx \left[H(j\omega_0) + \Delta\omega \frac{dH(j\omega)}{d\omega} \right] \tag{107}$$

The noise transfer function is

$$\left[\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)} \right] = \left[\frac{H(j\omega_0) + \Delta\omega \frac{dH(j\omega)}{d\omega}}{1 + H(j\omega_0) + \Delta\omega \frac{dH(j\omega)}{d\omega}} \right] \tag{108}$$

Since $H(j\omega_0) = -1$ and, for most practical case $\Delta\omega \frac{dH(j\omega)}{d\omega} \ll 1$, we can write

$$\left[\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)} \right] \approx \left[\frac{-1}{\Delta\omega \frac{dH(j\omega)}{d\omega}} \right] \tag{109}$$

From the noise transfer function, it appears that the noise component at $\omega = \Delta\omega + \omega_0$ is multiplied by the term $\left[\frac{-1}{\Delta\omega \frac{dH(j\omega)}{d\omega}} \right]$, relative to the output.

Therefore, the noise power spectral density can be explained as

$$\left|\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right|^2 = \left|\frac{-1}{\Delta\omega \frac{dH(j\omega)}{d\omega}}\right|^2 \tag{110}$$

for $H(j\omega) = A(j\omega)\exp[j\varphi(j\omega)]$ (111)

$$\frac{dH(j\omega)}{d\omega} = \left[\frac{dA(j\omega)}{d\omega} + jA(j\omega)\frac{d\varphi(j\omega)}{d\omega}\right]\exp[j\varphi(j\omega)] \tag{112}$$

Assume $\omega = \Delta\omega + \omega_0$ and $\omega \to \omega_0$, $|A(j\omega_0)| \to 1$, then the above equation is reduced to

$$\left|\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right|^2 = \left[\frac{1}{(\Delta\omega)^2 \left\{\left[\frac{dA(j\omega)}{d\omega}\right]^2 + \left[\frac{d\varphi(j\omega)}{d\omega}\right]^2\right\}}\right]_{\omega=\Delta\omega+\omega_0} \tag{113}$$

The open loop Q_L becomes

$$Q_L = \frac{\omega_0}{2}\sqrt{\left[\frac{dA(j\omega)}{d\omega}\right]^2 + \left[\frac{d\varphi(j\omega)}{d\omega}\right]^2} \tag{114}$$

and

$$\left|\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right|^2 = \left[\frac{1}{(\Delta\omega)^2 \left\{\left[\frac{dA(j\omega)}{d\omega}\right]^2 + \left[\frac{d\varphi(j\omega)}{d\omega}\right]^2\right\}}\right]_{\omega=\Delta\omega+\omega_0} = \frac{1}{4QL^2}\left[\frac{\omega_0}{\Delta\omega}\right]^2 \tag{115}$$

For the *LC* resonator $\left[\frac{dA(j\omega)}{d\omega}\right]$ at resonance ($\omega \to \omega_0$) becomes zero and $Q_L = \frac{\omega_0}{2}\frac{d\phi}{d\omega}$.
The broadband white noise is shaped by the resonator as seen in Fig. 24.

7.5   Non-unity Gain

For the non-unity gain feedback case, where $H(j\omega) = H_1(j\omega)H_2(j\omega)$ ([5, Eq. (8.1)] $S_{\Delta\phi}(\omega) = \frac{FkT}{P_s}$) it follows that

$$\left[\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right]_{\omega=\Delta\omega+\omega_0} \approx \left[\frac{-1}{\Delta\omega\left[\frac{dH(j\omega)}{d\omega}\right]}\right] \tag{116}$$
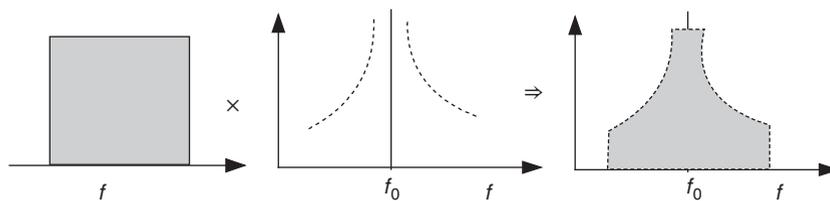
Figure 24   Noise shaping in the oscillator (Rohde et al. [5]/John Wiley & Sons).
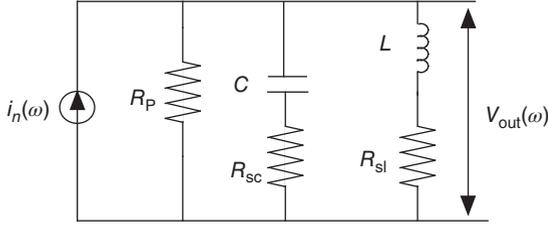
Figure 25 Noise response of the *RLC* resonator (Rohde et al. [5]/John Wiley & Sons).

and

$$\frac{Y_1(j\omega)}{X(j\omega)} = \frac{H_1(j\omega_0)}{1 + H(j\omega_0)} \tag{117}$$

then the noise power is shaped by the transfer function as

$$\left| \frac{Y_1(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)} \right|^2 = \frac{|H_1(j\omega)|^2}{(\Delta\omega)^2 \left| \frac{dH(j\omega)}{d\omega} \right|^2} \tag{118}$$

For the lossy resistor, inductor, capacitor (RLC) resonator, see Fig. 25.

Then,

$$H(\omega_0 + \Delta\omega) = \left[\frac{V_{\text{out}}(\omega_0 + \Delta\omega)}{i_n(\omega_0 + \Delta\omega)} \right]_{\omega = \Delta\omega + \omega_0} = \left[\frac{1}{g_{\text{resonator}}} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \left[\frac{1}{2Q_L} \right] \tag{119}$$

$$g_{\text{resonator}} = \frac{1}{R_P} \tag{120}$$

where R_P is the equivalent loss resistance of the resonator.

7.6 Noise Transfer Function and Spectral Densities

The noise transfer function for the relevant sources is

$$\text{NFT}_{\text{inr}}(\omega_0) = \frac{1}{2} \left[\frac{1}{2\omega_0 C_{\text{eff}}} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \rightarrow \tag{121}$$

The noise transfer function of the thermal loss resistance of the resonator.

$$\text{NFT}_{V_{bn}}(\omega_0) = \frac{1}{2} \left[\frac{C_1 + C_2}{C_2} \right] \left[\frac{1}{2Q} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \rightarrow \tag{122}$$

The noise transfer function of the transistor's base resistance noise.

$$\text{NFT}_{i_{bn}}(\omega_0) = \frac{1}{2} \left[\frac{C_2}{C_1 + C_2} \right] \left[\frac{1}{2\omega_0 Q C_{\text{eff}}} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \rightarrow \tag{123}$$

The noise transfer function of the transistor's base current flicker noise.

$$\text{NFT}_{ifn}(\omega_0) = \frac{1}{2} \left[\frac{C_2}{C_1 + C_2} \right] \left[\frac{1}{2\omega_0 Q C_{\text{eff}}} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \rightarrow \tag{124}$$

The noise transfer function of the transistor's flicker noise.

$$\text{NFT}_{i_{Cn}}(\omega_0) = \frac{1}{2} \left[\frac{C_1}{C_1 + C_2} \right] \left[\frac{1}{2\omega_0 Q C_{\text{eff}}} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \rightarrow \tag{125}$$

The noise transfer function of the collector current shot noise.
where

$$C_{\text{eff}} = C + \frac{C_1 C_2}{C_1 + C_2} \tag{126}$$

and

$$V_o(\omega_0) = n V_{be}(\omega_0) \tag{127}$$

$\text{NFT}_{in}(\omega_0)$, $\text{NFT}_{V_{bn}}(\omega_0)$, $\text{NFT}_{i_{bn}}(\omega_0)$, and $\text{NFT}_{i_{Cn}}(\omega_0)$ are the noise transfer functions as explained.

Figure 21a shows the four noise sources of the oscillator circuit whereby the flicker noise current is added to the base current and their noise spectral density is $\frac{K_f I_b^{AF}}{f_m}$.

$[\text{NSD}]_{inr} = \frac{4KT}{R_P}$ is the noise spectral density of the thermal noise current from the loss resistance of the resonator.

$[\text{NSD}]_{Vbn} = 4KTr_b$ is the noise spectral density of the thermal noise voltage from the base resistance.

$[\text{NSD}]_{ibn} = 2qI_b$ is the noise spectral density of the shot noise current from the base current.

$[\text{NSD}]_{ifn} = \frac{K_f I_b^{AF}}{f_m}$ is the noise spectral density due to $1/f$, where f is the flicker noise.

$[\text{NSD}]_{icn} = 2qI_c$ is the noise spectral density of the shot noise current from the collector current.

The phase-noise contribution now is

$$\text{PN}(\omega_0 + \Delta\omega) = [\text{NSD}]_{\text{noise-source}}[\text{NFT}_{\text{noise-source}}(\omega_0)]^2 \tag{128}$$

$$\text{PN}_{inr}(\omega_0 + \Delta\omega) = \frac{4KT}{R_P}[\text{NF}_{inr}(\omega_0)]^2 \tag{129}$$

$$\text{PN}_{Vbn}(\omega_0 + \Delta\omega) = 4KTr_b[\text{NF}_{Vbn}(\omega_0)]^2 \tag{130}$$

$$\text{PN}_{ibn}(\omega_0 + \Delta\omega) = 2qI_B[\text{NF}_{ibn}(\omega_0)]^2 \tag{131}$$

$$\text{PN}_{ifn}(\omega_0 + \Delta\omega) = \frac{K_f I_b^{AF}}{f_m}[\text{NF}_{ibn}(\omega_0)]^2 \tag{132}$$

$$\text{PN}_{icn}(\omega_0 + \Delta\omega) = 2qI_c[\text{NF}_{icn}(\omega_0)]^2 \tag{133}$$

where $\text{PN}(\omega_0 + \Delta\omega)$ is the phase noise at the offset frequency $\Delta\omega$ from the carrier frequency ω_0 and $[\text{NSD}]_{\text{noise-source}}$ is the noise spectral density of the noise sources.

The phase-noise contribution is

$\text{PN}_{inr}(\omega_0 + \Delta\omega) = \frac{4KT}{R_P}[\text{NFT}_{inr}(\omega_0)]^2 = \frac{4KT}{R_P}\left\{ \frac{1}{2}\left[\frac{1}{2\omega_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right] \right\}^2 \rightarrow$ phase-noise contribution from the resonator tank.

$\text{PN}_{Vbn}(\omega_0 + \Delta\omega) = 4KTr_b[\text{NFT}_{Vbn}(\omega_0)]^2 = 4KTr_b\left\{ \frac{1}{2}\left[\frac{C_1+C_2}{C_2}\right]\left[\frac{1}{2Q}\right]\left[\frac{\omega_0}{\Delta\omega}\right] \right\}^2 \rightarrow$ phase-noise contribution from the base resistance.

$\text{PN}_{ibn}(\omega_0 + \Delta\omega) = 2qI_b[\text{NFT}_{ibn}(\omega_0)]^2 = 2qI_b\left\{ \frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{\omega_0 QC_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right] \right\}^2 \rightarrow$ phase-noise contribution from the base current.

$\text{PN}_{ifn}(\omega_0 + \Delta\omega) = \frac{K_f I_b^{AF}}{f_m}[\text{NF}_{ibn}(\omega_0)]^2 = \frac{K_f I_b^{AF}}{f_m}\left\{ \frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{2\omega_0 QC_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right] \right\}^2 \rightarrow$ phase-noise contribution from the flicker noise of the transistor.

$\text{PN}_{icn}(\omega_0 + \Delta\omega) = 2qI_c[\text{NFT}_{icn}(\omega_0)]^2 = 2qI_c\left\{ \frac{1}{2}\left[\frac{C_1}{C_1+C_2}\right]\left[\frac{1}{2\omega_0 QC_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right] \right\}^2 \rightarrow$ phase-noise contribution from the collector current.

The total effect of all the four noise sources can be expressed as

$\text{PN}(\omega_0 + \Delta\omega) = [\text{PN}_{inr}(\omega_0 + \omega)] + [\text{PN}_{Vbn}(\omega_0 + \omega)] + [\text{PN}_{ibn}(\omega_0 + \omega)] + [\text{PN}_{icn}(\omega_0 + \omega)]$, [Ref. 5 Eq. (8.195)]

$$\text{PN}(\omega_0 + \Delta\omega) = \frac{4KT}{R_P}\left\{\frac{1}{2}\left[\frac{1}{2\omega_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 + 4KTr_b\left\{\frac{1}{2}\left[\frac{C_1 + C_2}{C_2}\right]\left[\frac{1}{2Q}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$$
$$+ \left[2qI_b + \frac{2\pi K_f I_b^{AF}}{\Delta\omega}\right]\left\{\frac{1}{2}\left[\frac{C_2}{C_1 + C_2}\right]\left[\frac{1}{2Q\omega_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$$
$$+ 2qI_c\left\{\frac{1}{2}\left[\frac{C_1}{C_1 + C_2}\right]\left[\frac{1}{2\omega_0 Q C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \qquad (134)$$

where
K_f is the flicker noise constant;
AF is the flicker noise exponent.

$$C_{\text{eff}} = C + \frac{C_1 C_2}{C_1 + C_2}$$

Note: The effect of the loading of the Q of the resonator is calculated by the noise transfer function multiplied with the noise sources.

The phase-noise contribution from the different noise sources for the parallel-tuned Colpitts oscillator circuit at $\Delta\omega = 10\,\text{kHz} \cdot 2\pi$ from the oscillator frequency $\omega_0 = 100\,\text{MHz} \cdot 2\pi$ will now be computed.

Circuit parameters:
Base resistance of transistor $r_b = 6.14\,\Omega$.
Parallel loss resistance of the resonator $R_P = 7.5\text{E}11\,\Omega$.
Our 100 MHz case
Q of the resonator $= 60{,}000$.
Resonator inductance $= 15\,\text{mH}$.
Resonator capacitance $= 2.7\,\text{pF}$.
Collector current of the transistor $I_c = 13\,\text{mA}$.
Base current of the transistor $I_b = 130\,\mu\text{A}$.
Flicker noise exponent $AF = 2$.
Flicker noise constant $K_f = 1\text{E-}11$.
Feedback factor $n = 6$.
Comparing phase noise at 100 Hz and phase noise at 10 kHz.

Phase noise @ 100 Hz:	Phase noise @ 10 kHz:
$\text{PN}_{inr}(\omega_0 + 100\,\text{Hz}) = -162\,\text{dBc/Hz}$	$\text{PN}_{inr}(\omega_0 + 10\,\text{kHz}) = -202\,\text{dBc/Hz}$
$\text{PN}_{Vbn}(\omega_0 + 100\,\text{Hz}) = -176\,\text{dBc/Hz}$	$\text{PN}_{Vbn}(\omega_0 + 10\,\text{kHz}) = -216\,\text{dBc/Hz}$
$\text{PN}_{(ibn + ifn)}(\omega_0 + 100\,\text{Hz}) = -140\,\text{dBc/Hz}$	$\text{PN}_{(ibn + ifn)}(\omega_0 + 10\,\text{kHz}) = -200\,\text{dBc/Hz}$
$\text{PN}_{(icn)}(\omega_0 + 100\,\text{Hz}) = -148\,\text{dBc/Hz}$	$\text{PN}_{(icn)}(\omega_0 + 10\,\text{kHz}) = -189\,\text{dBc/Hz}$

Note: The noise contribution from the resonator at this offset is the same as the flicker noise contribution from the transistor.

It appears that the flicker noise and the noise from the resonator are the limiting factors for the overall phase-noise performance of the oscillator circuit.

The dependence of the phase-noise performance due to different noise sources present in the oscillator circuits is

$$PN_{imr}(\omega_0 + \Delta\omega) \propto \frac{1}{R_p} \tag{135}$$

$$PN_{Vbn}(\omega_0 + \Delta\omega) \propto = r_b \left\{ \frac{1}{Q} \left[1 + \frac{C_1}{C_2} \right] \right\}^2 \tag{136}$$

$$PN_{ibn}(\omega_0 + \Delta\omega) \propto I_b \left\{ \frac{1}{QC_{\text{eff}}} \left[\frac{C_2}{C_1 + C_2} \right] \right\}^2 \tag{137}$$

$$PN_{icn}(\omega_0 + \Delta\omega) \propto = I_c \left\{ \frac{1}{QC_{\text{eff}}} \left[\frac{C_1}{C_1 + C_2} \right] \right\}^2 \tag{138}$$

Once the resonator Q is known (parallel loss resistance is fixed), then the only option left is to select a device having a low flicker noise. The base resistance, current, and collector current add little to the performance! Finally, optimization of the phase noise can be done by proper selection of the feedback capacitor under the constraints of the loop gain so that it maintains oscillation.

The value of "n" is defined as $(1 + C_1/C_2)$. Table 3 shows the resulting phase noise of a 100 MHz crystal oscillator.

The combined phase noise, a result of all the noise contributions, depends on the semiconductor, the resonator losses, and the feedback capacitors. Figure 26 shows the simulated phase noise for a given set of semiconductor parameters and various levels of n. While the values for $n = 1.5$ and 2 provide similar results and converge for frequencies more than 1 MHz off the carrier, the results for $n = 3$ also provide a much noisier condition, even at far-out frequencies. The reason is the reduced output power and a heavier loading of the resonator.

Need introductory write up explaining Figs. 27 and 28a,b.

In order to obtain oscillation, the circuit shown in Fig. 27 generates a negative resistance to compensate the losses of the crystal (70 Ω). Initially, the value of this negative resistance has to be larger than the loss resistor (e.g., −200 Ω) and then the steady-state value of the resistor has to be slightly more negative than the 70 Ω.

Important: This electronic resistance is noisy from the noise contribution of the transistor. One can assume that the transistor is noise free, and all the noise sources are in this negative resistance.

The capacitance ratio based on an open loop gain of 6 and calculations of Y_{21} (0.225) and the DC (100 mV) offset based on the Bessel function is 6.

The simulation confirms that oscillation occurs at the correct frequency and the phase noise, see Fig. 28.

Figure 28b shows a measured phase-noise plot of a 100 MHz crystal oscillator [33].

A comment: Figure 29 showing a time-domain simulation of the 100 MHz oscillator indicates that the maximum collector current in this design is exceeded (60 mA). A change to a BFR96 transistor cured this problem.

Table 3 Phase Noise as a Function of Feedback Factor *n*

$n = (1 + C_1/C_2)$	Resulting PN at 100 Hz (dBc/Hz)	Resulting PN at 10 kHz (dBc/Hz)
2	−130	−190
3	−136	−193.4
4	−140	−193.4
5	−142	−193.4
6	−144	−193.4
7	−146	−193.4

$n = R_p \times Y_{21}/LG$; large signal loop gain = 5

$I_{dc} = 15$ mA

$Y_{21} = 15$ mS $\times 1.7/0.1$ ($x = 6$) $= 0.255$ mS

$R_p = 2 \times R_s$ (Crystal)

$n = 144 \times 0.255/5 = 7.3$

$C_1/C_2 = n - 1 = 6$; 120 pf/20 pf = 6
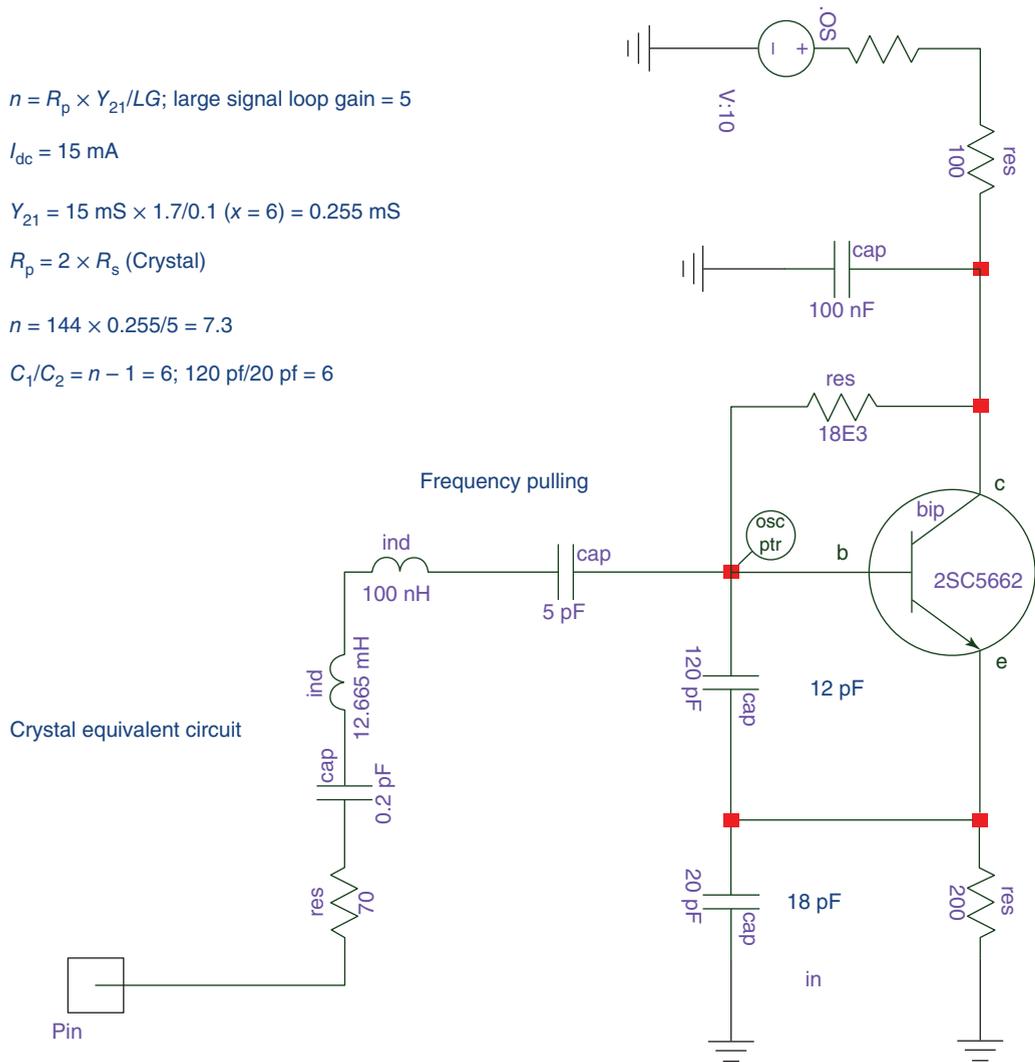
Figure 27 Negative impedance calculation (Rohde and Apte [33]/IEEE).

Assuming that we are designing the bias circuit to provide a certain device bias current I_c and collector voltage V_c, select a convenient supply voltage $A^+ > V_c$. The component values are then supplied by the following equations:

$$R_c = \frac{A^+ - V_c}{I_c} \tag{141}$$

$$R_1 = \frac{A^+ - V_c}{I_d} \tag{142}$$

$$R_2 = \frac{V_c - V_d}{I_d} \tag{143}$$

$$R_b < \beta \frac{V_c - V_d - 0.2}{I_c}\bigg|_{min} \tag{144}$$
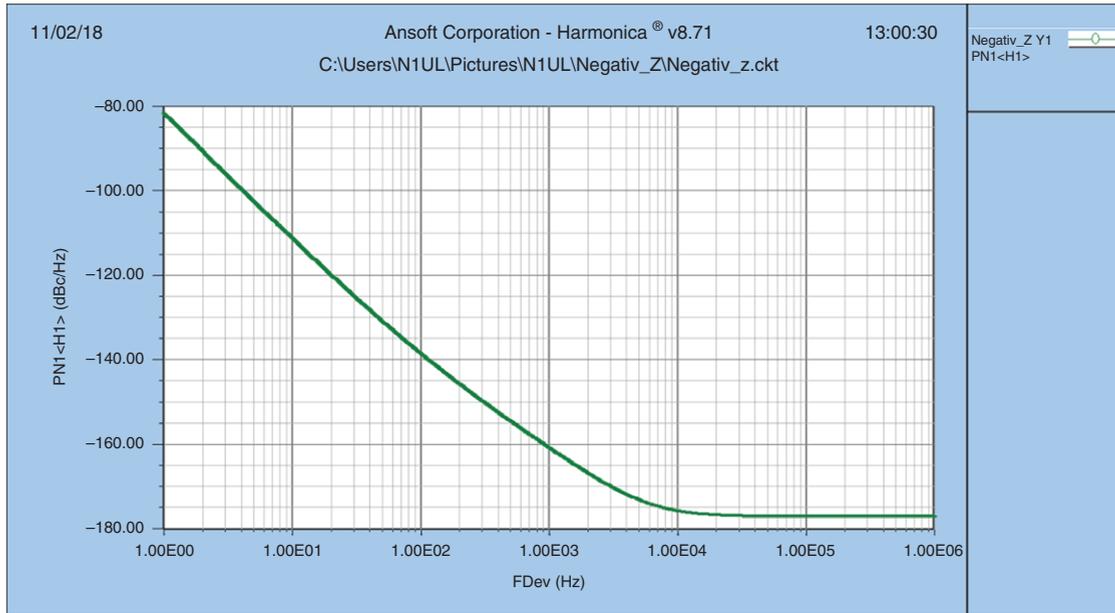
(a)
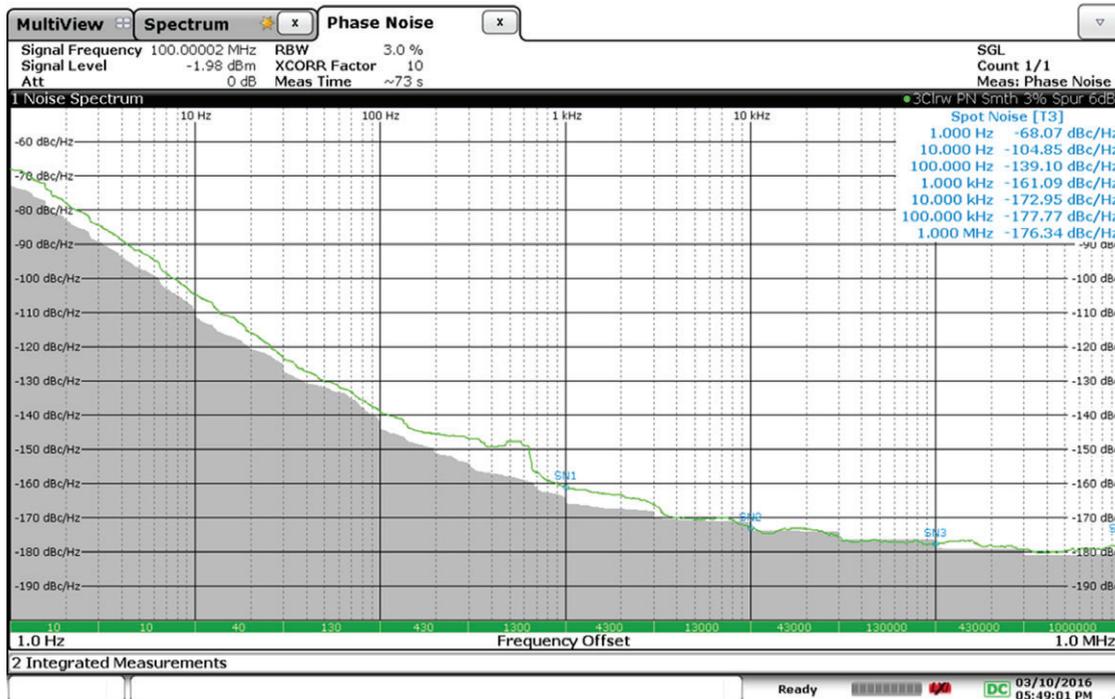
(b)

Figure 28 (a) Simulated phase-noise plot of the circuit in Fig. 27. (b) Measured phase-noise plot of a 100 MHz crystal oscillator (Rohde and Apte [33]/IEEE).
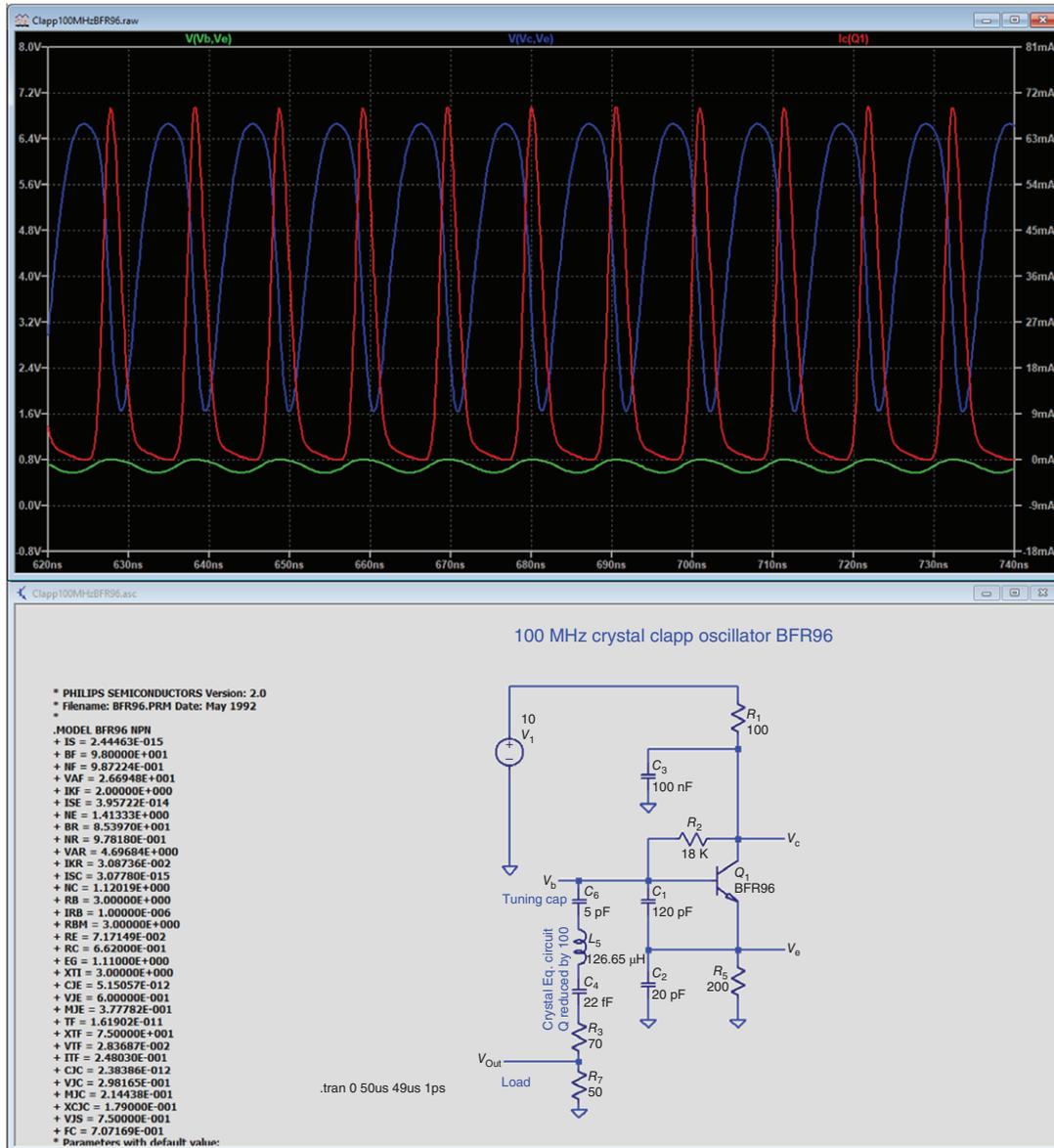
Figure 29 A time-domain simulation of the 100 MHz oscillator indicates that the maximum collector current in this design is exceeded (60 mA). A change to a BFR96 transistor cured this problem.

I_c is the desired collector current of Q_1 (A);

V_c is the desired collector voltage of Q_1 (V);

V_d is the diode, or base–emitter voltage drop, nominally 0.7 (V);

A^+ is the chosen supply voltage (V);

R_i are resistor values as shown in Fig. 30 (Ω);

I_d is the bias current through R_1, R_2, and D_1 (A);

β_{min} is the minimum beta of Q_1.
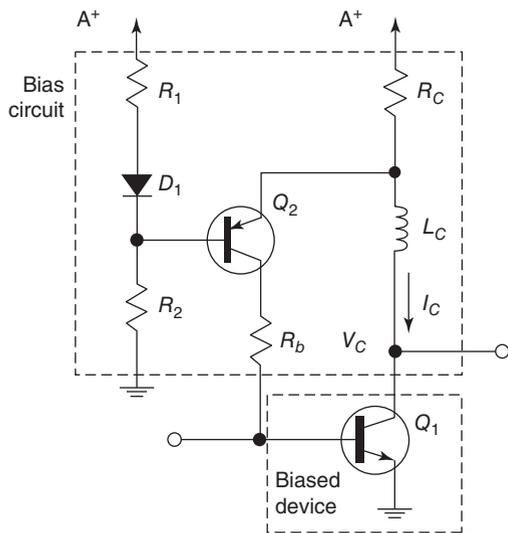
Figure 30 Active bias network for a common-emitter RF amplifier stage (Rohde et al. [5]/John Wiley & Sons).
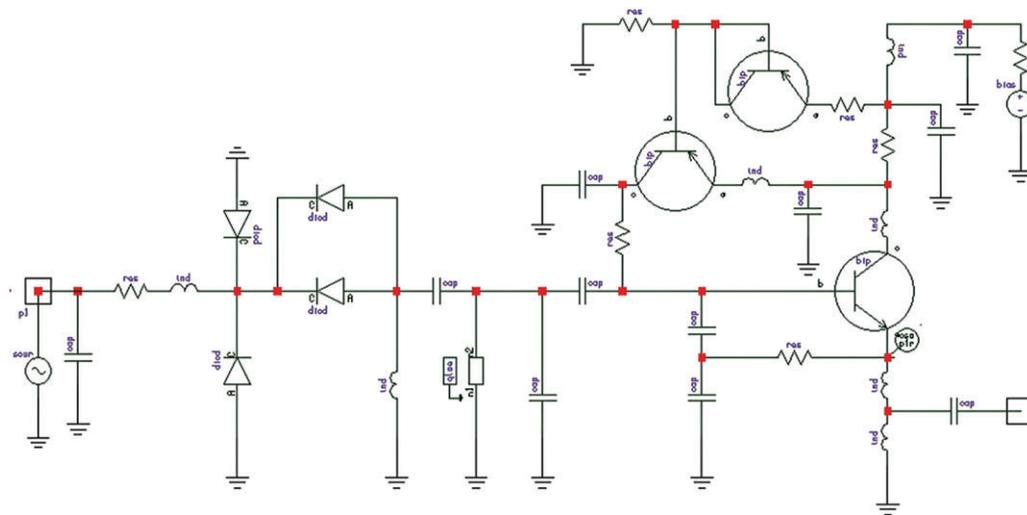
Figure 31 1000 MHz ceramic resonator oscillator (Rohde et al. [5]/John Wiley & Sons).

The bias circuit shown has to be carefully bypassed at both high and low frequencies. There is one inversion from base to collector of Q_1, and another inversion may be introduced by L_c matching components and stray capacitances, resulting in positive feedback around the loop at low frequencies. Low equivalent series resistance (ESR) electrolytic or tantalum capacitors from the collector of Q_2 to ground are usually adequate to ensure stability.

The ceramic resonator is coupled loosely to the transistor with a capacitor of 0.9 pF. The resonator has a parallel capacitor of 0.6 pF, which reduces the manufacturing tolerances of the resonator. The tuning diode assembly, two diodes in parallel, is coupled to the resonator with 0.8 pF. The reason for using two diodes was that there was not one single diode available with the necessary capacitance and Q. Figure 31 shows the schematic of the oscillator.

It has been pointed out that the best operating condition will be the case where the most negative resistance occurs at the point of resonance to achieve the best phase noise. This is shown in Fig. 32. The purple-colored
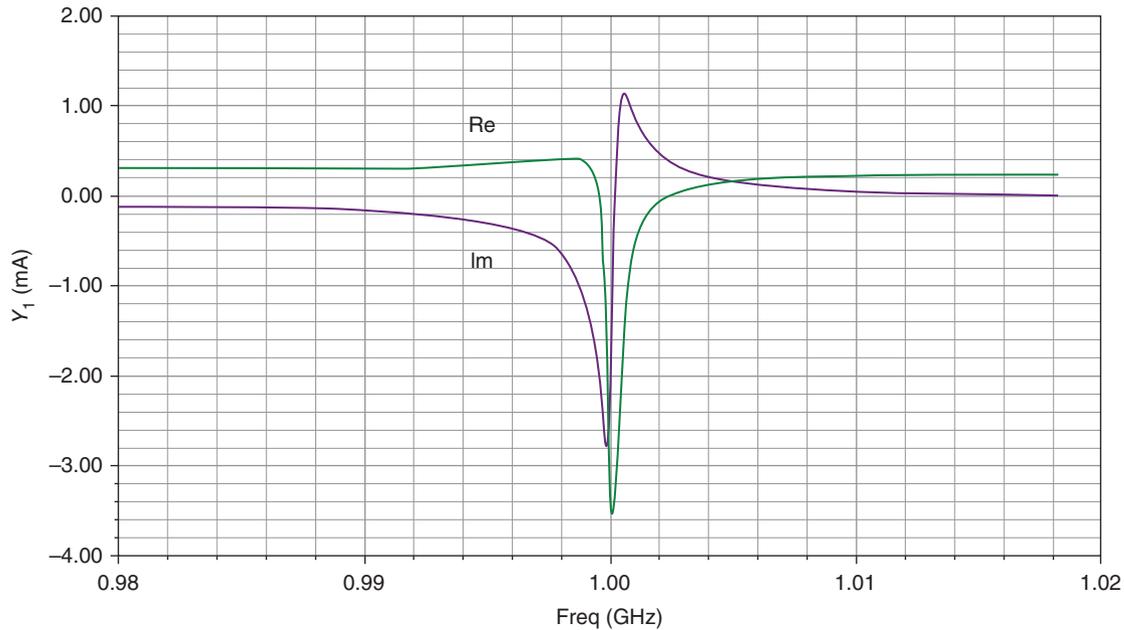
Figure 32 Plot of the real and imaginary oscillator currents as a function of frequency (Rohde et al. [5]/John Wiley & Sons).

curve starting below zero shows the imaginary current which resonates at 1000 MHz, while the green-colored curve shows the negative resistance. Its maximum negative peak occurs at exactly 1000 MHz, as it should be.

Figure 33 shows the measured phase noise of this oscillator. The measurements were performed with the Aeroflex Euro Test system. At 1 kHz, the phase noise is approximately 95 dBc/Hz and, at 10 kHz, it is approximately 124 dBc/Hz. This is a 30 dB/decade slope, which is triggered by the flicker corner frequency of the transistor. From 10 to 100 kHz, the slope is 20 dB/decade with a phase noise of −145.2 dBc/Hz at 100 kHz. At 1 MHz off the carrier, it is −160 dBc/Hz.

Because of the narrow tuning range and the loose coupling of the tuning diode, the noise contribution of the diode is negligible.

This circuit has been designed using the synthesis procedure and also has been analyzed with the harmonic-balance simulator *Microwave Harmonica* from Ansoft Corporation. Figure 34 shows the predicted performance of the phase noise. The actual circuit arrangement is shown in Fig. 35. The ceramic resonator can be spotted easily.

9 4100 MHz OSCILLATOR WITH TRANSMISSION LINE RESONATORS

For less demanding applications, it is possible to design oscillators using transmission line resonators. As discussed in Ref. 5, chap. 5, *Q* of the transmission line resonators depends on the material and implementation of the resonator. Figure 36 shows the circuit of the oscillator. While the previous example was a Colpitts parallel resonant circuit, this circuit operates in series resonant mode. The NPN transistor NE68830 has parasitic inductance in the emitter, base, and collector lines. For the purpose of accurate modeling, T-shaped (TEE) and cross-junction models were used, as well as transmission lines where applicable. The DC stabilization circuit uses the same technique as shown in Fig. 31. This time the RF power is taken from the collector and uses a 10 dB attenuator to minimize frequency pulling. The ground connections for the capacitors are done using via holes. A via hole is the electrical equivalent of a small inductor.
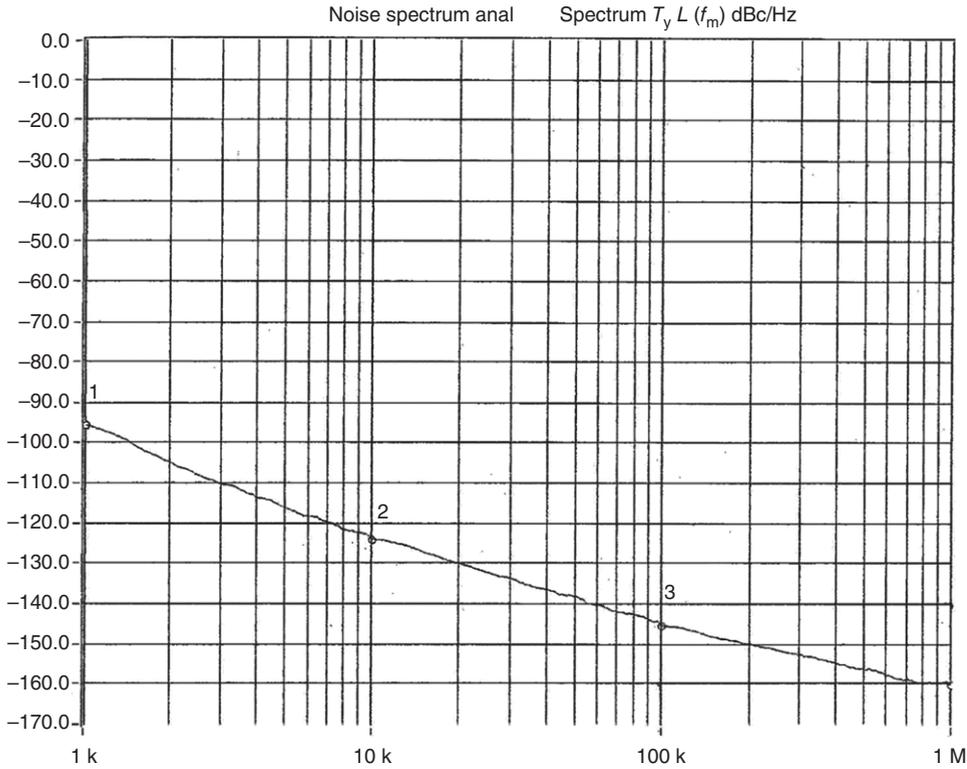
Figure 33 Measured phase noise of the 1000 MHz ceramic resonator oscillator (Rohde et al. [5]/John Wiley & Sons).

$X_1 = 1.00\text{E}03$ Hz $X_2 = 1.00\text{E}06$ Hz
$Y_1 = -96.30$ dBc/Hz $Y_2 = -160.67$ dBc/Hz
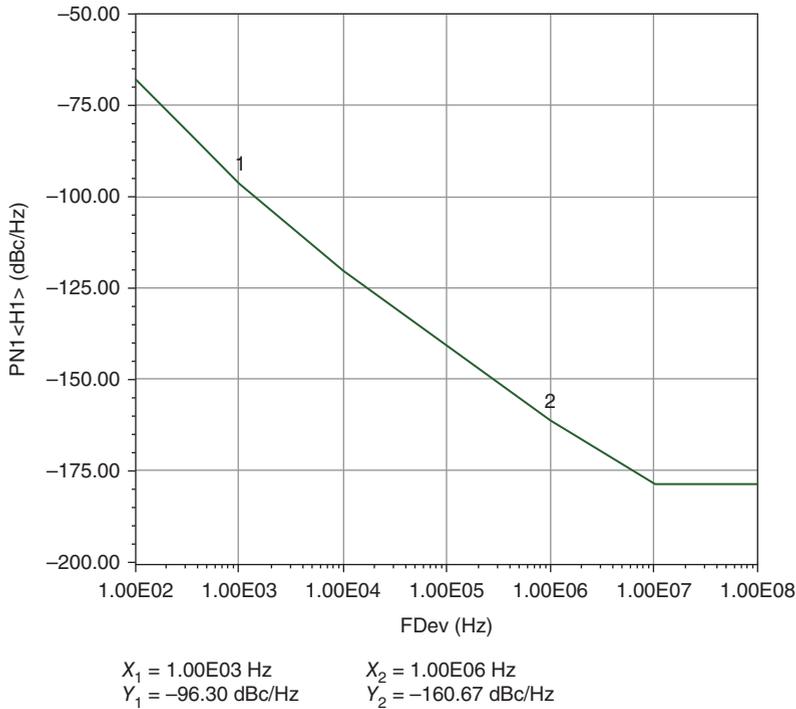
Figure 34 Predicted phase noise of the CRO at 1 GHz shown in Fig. 31 (Rohde et al. [5]/John Wiley & Sons).

Figure 35 Photograph of the 1 GHZ CRO of the schematic shown in Fig. 31 (Rohde et al. [5] from John Wiley & Sons).
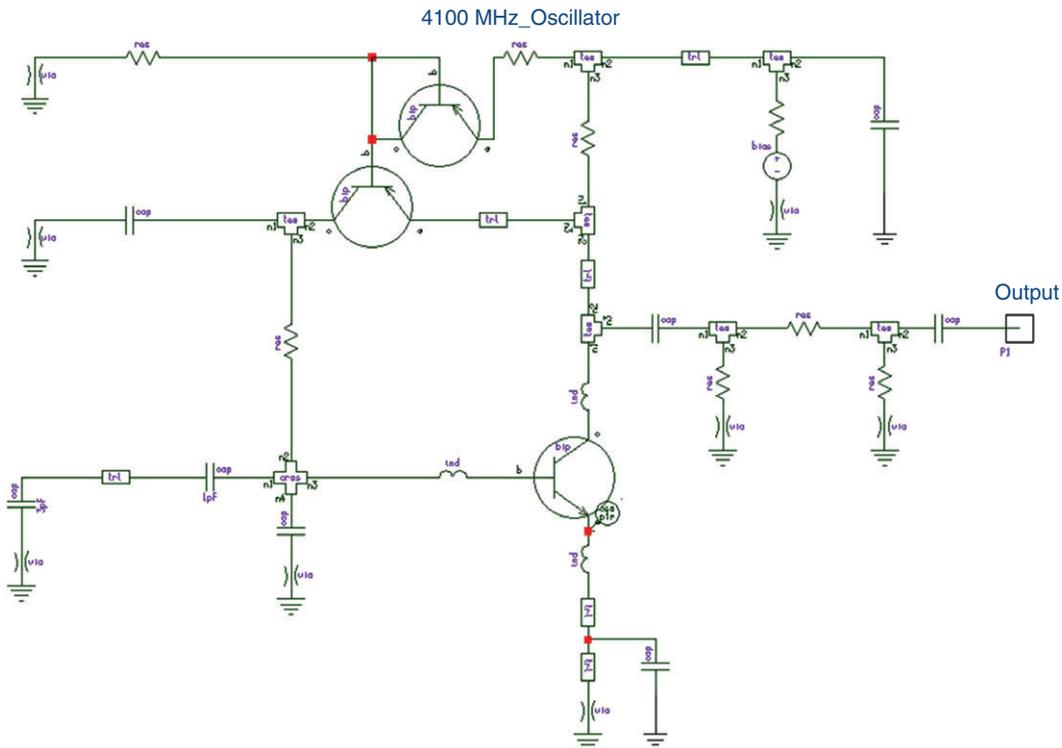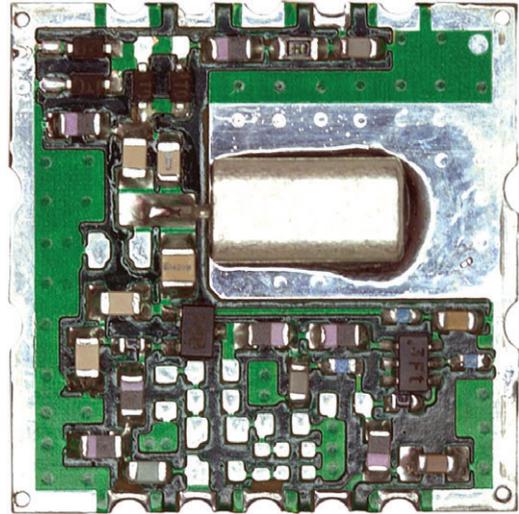
Figure 36 Circuit diagram of the 4.1 GHz oscillator (Rohde et al. [5]/John Wiley & Sons).

The phase noise of this oscillator was simulated using the values of the synthesis program. Figure 37 shows the predicted phase noise.

The output power of this oscillator is 6.8 dBm. This oscillator was built and measured. Figure 38 shows the printed circuit board of the oscillator.

Because of the pad-like microstrips, the simulation needs to be done very carefully, and the soldering of the component is also very critical. This frequency range makes the assembly very difficult because it is not high

Phase noise @ 100 KHz = −116 dBc/Hz
Osicllator frequency = 4100 MHz

X_1 = 1.00E05 Hz
Y_1 = −116.17 dBc/Hz
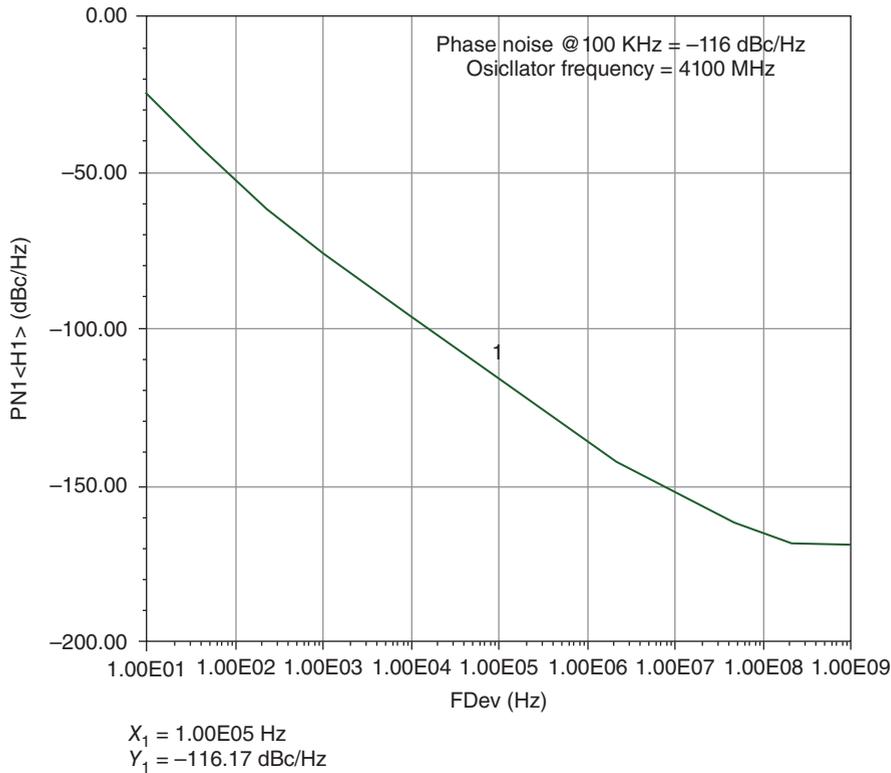
Figure 37 Predicted phase noise of the 4.1 GHz oscillator (Rohde et al. [5]/John Wiley & Sons).
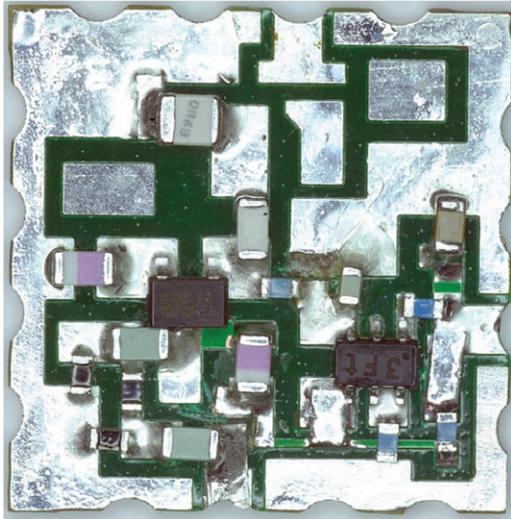
Figure 38 Printed circuit board of the 4.1 GHz oscillator shown in Fig. 37 (Rohde et al. [5] from John Wiley & Sons).

enough for an radio frequency integrated circuit (RFIC) and still needs to be done on a printed circuit board. The measured phase noise is shown in Fig. 39. It agrees well with the predicted phase noise. At 100 kHz, the difference is about 3 dB. The same is valid at 10 kHz. At 1 kHz, there is a larger difference. The flicker corner frequency of the actual device is different than the simulation.

Noise spectrum anal   Spectrum T_y $L(f_m)$ dBc/Hz
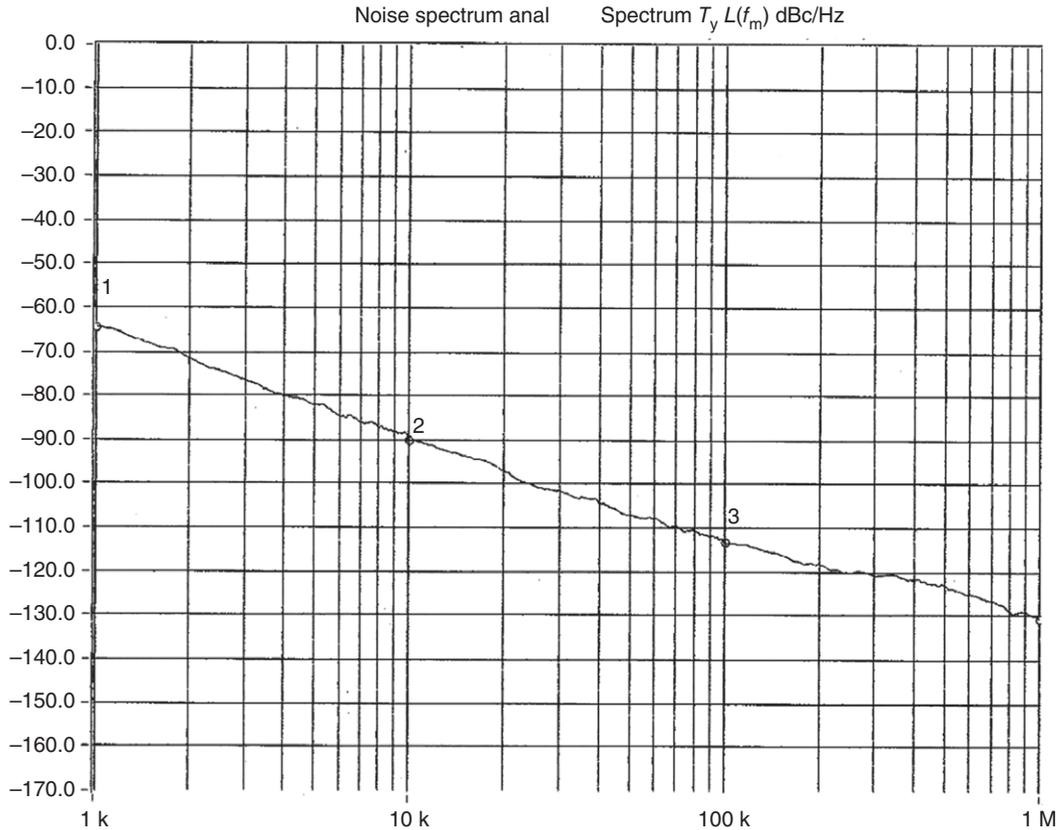
Figure 39   Measured phase noise of the 4.1 GHz oscillator (Rohde et al. [5]/John Wiley & Sons).

10   2000 MHz GaAs FET-BASED OSCILLATOR

Low-cost applications are frequently implemented as an RFIC. For further validation, a GaAs FET-based 2000 MHz Colpitts oscillator was designed and built. Figure 40 shows the circuit diagram of the oscillator. It uses a combination of transmission lines and rectangular inductors as resonators. The inductor in the middle of the schematic in Fig. 40, connected to a via hole, is needed as a DC return. If a tuning diode is connected to the capacitor on the left of the schematic in Fig. 40, then a DC control voltage can be applied, and the center inductor becomes an RF choke. The output is taken from the source. An additional external DC decoupling capacitor will be needed because of the DC coupling. The transistor and the circuit were constructed using the TriQuint GaAs Foundry and the transistor was optimized for the DC current. Figure 41 shows the predicted phase noise of this oscillator.

The measured values were 100 dBc/Hz at 100 kHz and 120 dBc/Hz at 1 MHz. There is a deviation of about 2 dB compared to simulation [5].

It is interesting to examine the load line of this oscillator, which is shown in Fig. 42. This circuit is operated in a fairly linear range.

Figure 43 shows the layout of the 2 GHz GaAs FET oscillator. Its output power is 1.8 dBm.
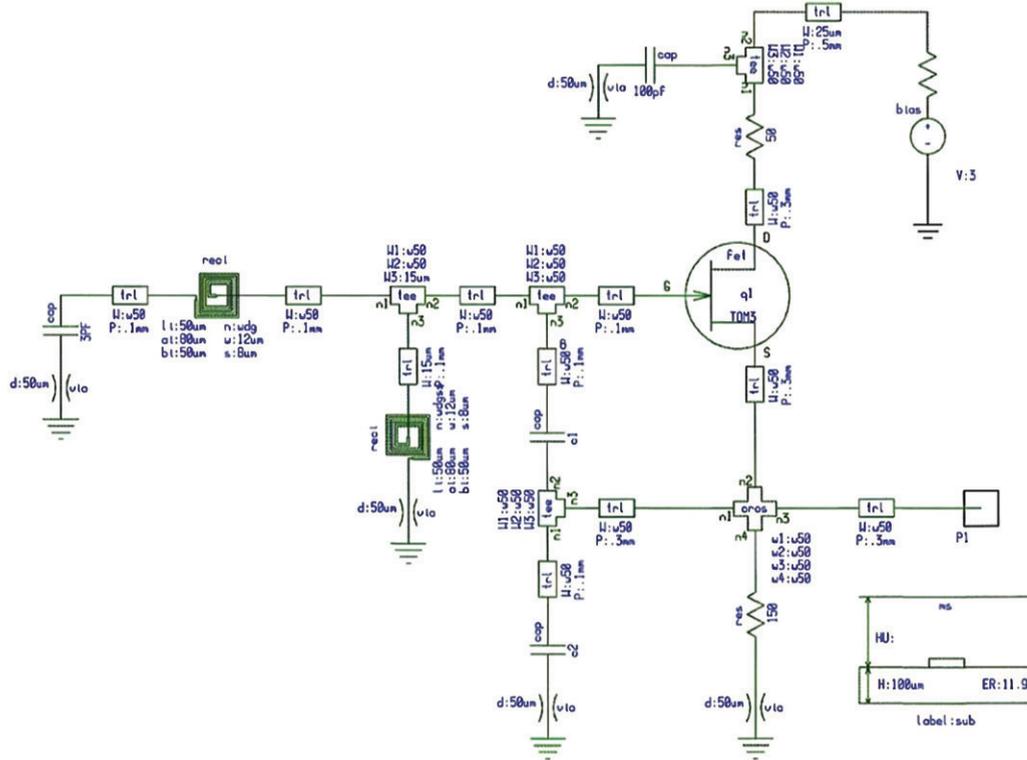
Figure 40 Circuit diagram of the 2 GHz GaAs FET oscillator (Rohde et al. [5]/John Wiley & Sons).

11   77 GHz SiGe OSCILLATOR

Millimeter wave oscillators have been published using SiGe bipolar transistors. A lot of data on output power and phase noise regarding these oscillators is found in literature. Therefore, it was interesting to synthesize a 77 GHz oscillator using lossy, lumped elements, which later can be translated into distributed elements, specifically, coplanar waveguides.

Figure 44 shows a Colpitts oscillator which is designed around an advanced product of the BFP620 family. It is the typical Colpitts arrangement with a capacitive divider. The resonant circuit consists of a 0.07 pF capacitor and a 100 pH inductor with a Q of 70. Figure 45 shows the predicted phase noise at 77 GHz, which agrees well with published data. Here, $n = \left(1 + 1\frac{C_1}{C_2}\right) = 3$ (low Q case as described earlier!). The literature shows that such values are obtainable! [5, 38, 39].

12   900–1800 MHz HALF-BUTTERFLY RESONATOR-BASED OSCILLATOR

This is the example of an oscillator which can only be analyzed, built, and optimized using electro magnetic (EM) tools. The resonator here is a quarter-wave length resonator at 1800 MHz, which gets pulled down by the tuning diodes. Its schematic is shown in Fig. 46.

$X_1 = 1.00E05$ Hz $X_2 = 1.00E06$ Hz $X_3 = 1.00E07$ Hz
$Y_1 = -98.04$ dBc/Hz $Y_2 = -122.22$ dBc/Hz $Y_3 = -142.68$ dBc/Hz
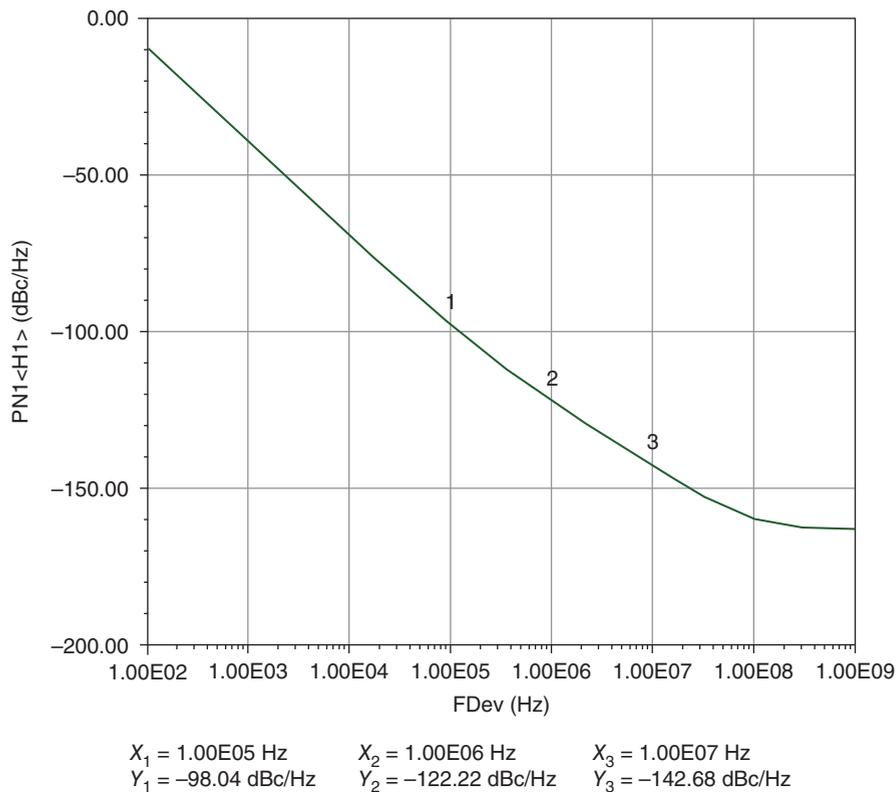
Figure 41 Predicted phase noise of the oscillator shown in Fig. 40.
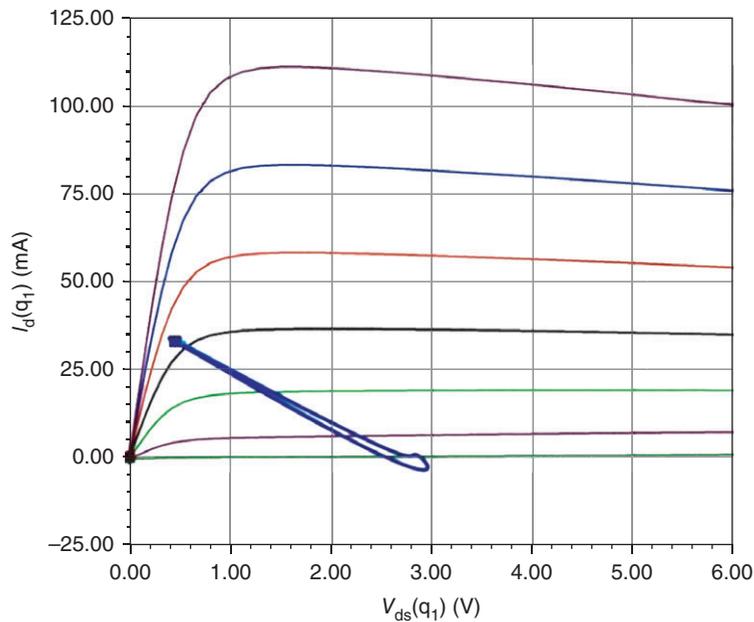
Figure 42 The DC-IV and the load line for the GaAs FET oscillator [5] are shown (Rohde et al. [5]/John Wiley & Sons).
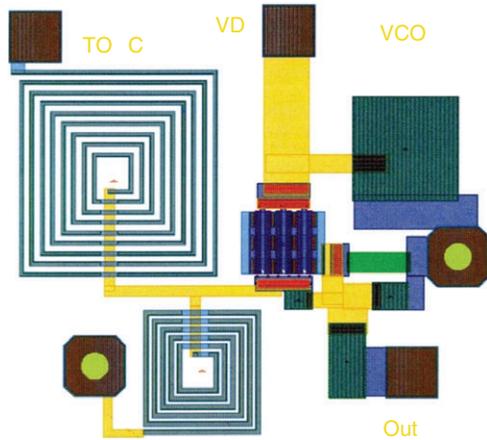
Figure 43 Layout of the 2 GHz GaAs FET oscillator (Rohde et al. [5]/John Wiley & Sons).
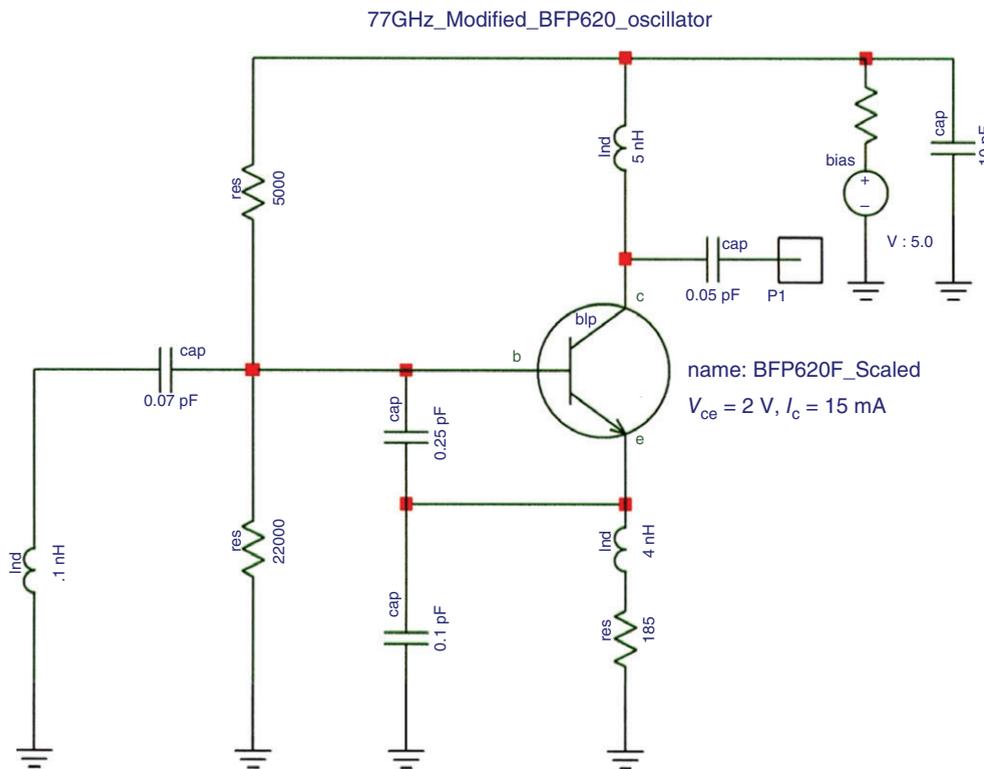
Figure 44 77 GHz Colpitts oscillator (Rohde et al. [5]/John Wiley & Sons).

For a better understanding of the circuit, which highly depends upon the layout information is given in Fig. 47. The resonator is shown on the top right of the layout, a half-butterfly arrangement. The hole on the lower right side is the marking for the ground via.

This was the first attempt to build an EM-based oscillator from where the coupled resonator activity evolved. Figure 47 shows the actual built oscillator, and Fig. 48 shows the achieved phase noise. Given the fact that this
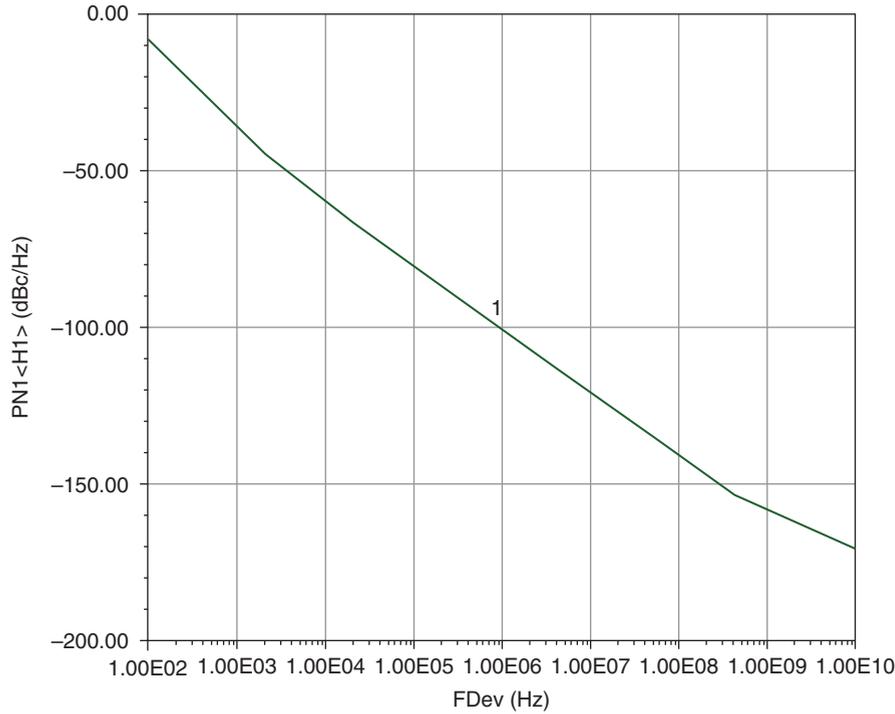
X_1 = 1.00E06 Hz
Y_1 = −100.43 dBc/Hz

Figure 45 Predicted phase noise of the oscillator shown in Fig. 44 (Rohde et al. [5]/John Wiley & Sons).

is a 1–2 range oscillator (900–1800 MHz), the phase noise compares favorably with other efforts in this frequency range.

12.1 Coupled Resonator

The Q factor of the resonator can be increased by introducing the coupling factor β, which is defined as the ratio of the series coupling capacitor to the resonator capacitor. Figure 49a shows two identical resonators with series coupling where Z_r and Z_c are the resonators and the coupling network impedance, respectively.

The effective coupled impedance of Ref. 5, figure 10.41 shown here as Fig. 49b is given by

$$Z_{\text{eff}}(\omega) = \left[\frac{V_o}{I_{in}}\right] = \frac{Z_r(\omega)}{2 + \frac{Z_c(\omega)}{Z_r(\omega)}} = \frac{Z_r^2(\omega)}{Z_c(\omega) + 2Z_r(\omega)} \tag{145}$$

where I_{in} is the large-signal current from the active device.

$$Y_{\text{eff}}(\omega) = \frac{1}{Z_{\text{eff}}(\omega)} = \left[\frac{Z_c(\omega)}{Z_r^2(\omega)} + \frac{2}{Z_r(\omega)}\right] = \left[\frac{Y_r^2(\omega)}{Y_c(\omega)} + 2Y_r(\omega)\right] \tag{146}$$

For $Z_c(\omega) \gg Z_r(\omega)$, and assuming the Q factor of $Z_r(\omega)$ is sufficiently large, the denominator of equation (10.305) may be considered constant over the frequencies within the bandwidth of $Z_r(\omega)$. The coupling admittance is defined by $Y_c(\omega) = j\omega C_c$.

Figure 46 Schematic of the oscillator used to demonstrate the multiple-coupled resonator. Its technique is described in Rohde et al. [5], Chapter 10/John Wiley & Sons.

Figure 47 Photograph of the 900–1800 MHz voltage Controlled Oscillator (VCO) (Rohde et al. [5] from John Wiley & Sons).
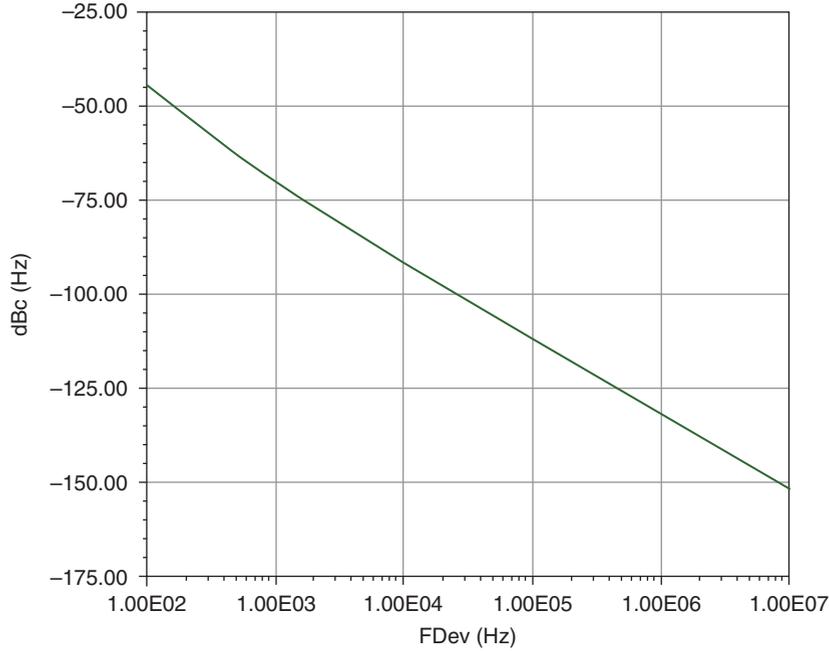
Figure 48 Predicted phase noise of the half-butterfly resonator oscillator (Rohde et al. [5]/John Wiley & Sons).

The resonator admittance is given by

$$Y_r(\omega) = \left[\frac{1}{R_P} + \frac{1}{j\omega L} + j\omega C \right] = \left[\frac{j\omega L R_P}{R_P(1 - \omega^2 LC) + j\omega L} \right]^{-1} \tag{147}$$

From (146) and (147), $Y_{eff}(\omega)$ can be rewritten as

$$Y_{eff}(\omega) = \left[\frac{2}{R_P} - \frac{2R_P(1 - \omega^2 LC)}{\omega^2 L R_p^2 \beta C} \right] + j \left[\frac{\left[R_P^2(1 - \omega^2 LC)^2 - \omega^2 L^2 \right]}{\omega^3 R_P^2 L^2 \beta C} - \frac{2R_P(1 - \omega^2 LC)}{R_P \omega L} \right] \tag{148}$$

From (147), the phase shift of the coupled resonator is given as

$$\phi = \tan^{-1} \left[\frac{\left(\frac{\left[R_P^2(1 - \omega^2 LC)^2 - \omega^2 L^2 \right]}{\omega^3 R_P^2 L^2 \beta C} - \frac{2R_P(1 - \omega^2 LC)}{R_P \omega L} \right)}{\left(\frac{2}{R_P} - \frac{2R_P(1 - \omega^2 LC)}{\omega^2 L R_p^2 \beta C} \right)} \right] \tag{149}$$

At resonance, the real part of $Y_{eff}(\omega)$ is reduced to zero, and the resonance frequency can be derived as

$$Re[Y_{eff}(\omega)]_{\omega=\omega_0} = \left[\frac{2}{R_P} - \frac{2R_P(1 - \omega^2 LC)}{\omega^2 L R_p^2 \beta C} \right]_{\omega=\omega_0} = 0 \Rightarrow \omega_0^2 LC(1 + \beta) = 1 \tag{150}$$

$$[\omega_0]_{\varphi=90°} = \frac{1}{\sqrt{LC(1 + \beta)}} \tag{151}$$

$$[Y_{eff}(\omega)]_{\omega=\omega_0} = -j \left[\frac{\left[R_P^2 \beta^2 C + (1 + \beta)L \right]}{\beta(1 + \beta)\omega L R_P^2 C} \right] \tag{152}$$
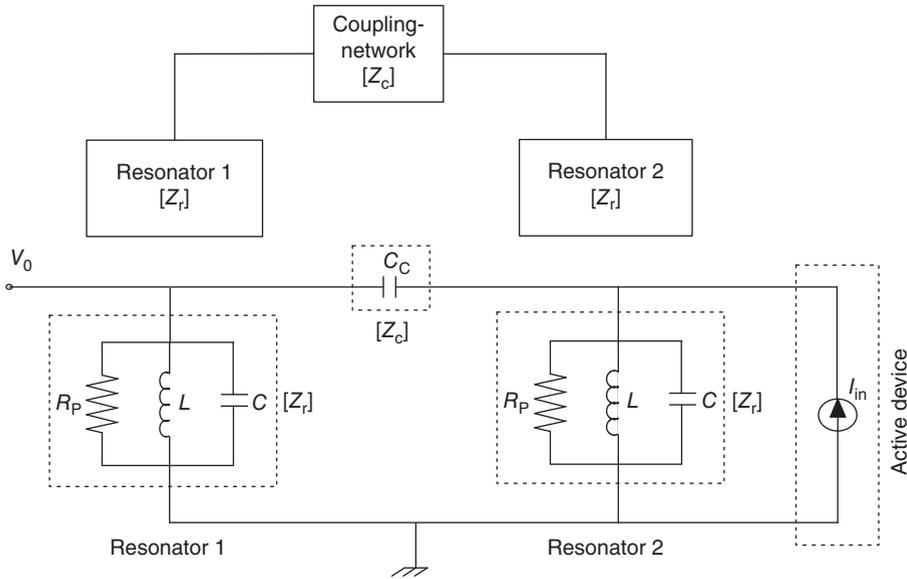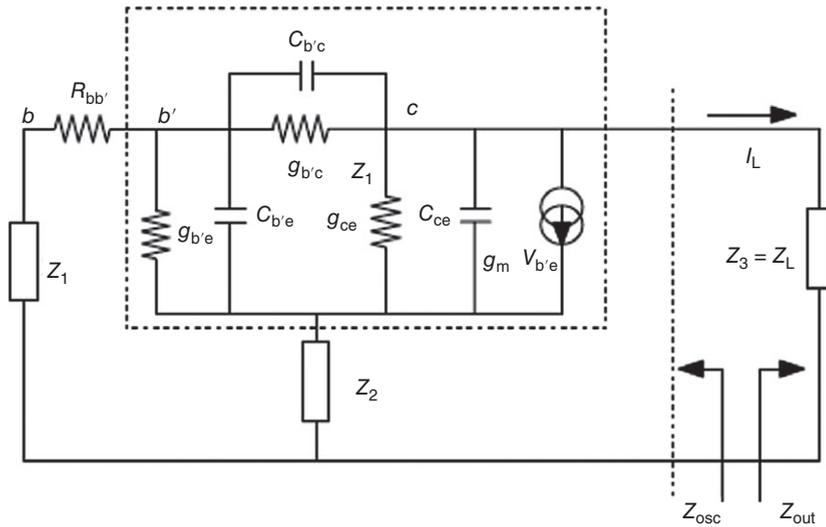
Figure 49 (a) Series capacitive coupled resonator (Rohde et al. [5]/John Wiley & Sons). (b) Series feedback topology of the oscillator using a bipolar transistor.

$$[Z_{\text{eff}}(\omega)]_{\omega=\omega_0} = j \left[\frac{\beta(1+\beta)\omega L R_p^2 C)}{R_p^2 \beta^2 C + (1+\beta)L} \right] = j \left[\frac{\beta R_P^2 \omega C}{\frac{R_p^2 \beta^2 C}{(1+\beta)L} + 1} \right] \Rightarrow j \left[\frac{Q_0 \beta R_P}{1 + Q^2 \beta^2} \right]$$

(153)

where $Q_0 = \omega C R_P = \frac{R_P}{\omega L}$; $\beta = \frac{C_c}{C}$

From (151), the effective quality factor of the coupled resonator is given by [40–42]

$$[Q_{\text{eff-coupled}}(\omega_0)]_{\omega=\omega_0} = \frac{\omega_0}{2} \left[\frac{\partial \phi}{\partial \omega} \right] \Rightarrow \left[\frac{2Q_0(1+\beta)}{\left(1 + Q_0^2 \beta^2\right)} \right]$$

(154)

$$[Q_{\text{eff-coupled}}(\omega_0)]_{\beta \ll 1} = \left[\frac{2Q_0(1+\beta)}{(1+Q_0^2\beta^2)} \right]_{\beta \ll 1} \approx 2Q_0 \tag{155}$$

Weakly coupled resonators ($\beta \ll 1$) will produce high attenuation due the large value of Z_c, so a trade-off between doubling the Q factor and the permissible attenuation is required for the best phase-noise performance. For octave-band tunability, the coupling factor, β, is dynamically adjusted over the tuning range for low-noise performance.

12.2 Optimum Phase Noise with Respect to the Loaded Q

The amount of loading on a resonator is critical for optimum phase noise in VCOs. A very lightly loaded resonator will have a higher Q factor but will pass less power through it whereas a heavily loaded resonator will have a very low Q factor but will pass more power through it. From Fig. 50, the equivalent loading is R_{reso} in parallel with the series combination of $1/g_m$ and R_L and this will represent the loading factor in the oscillator circuit.

From Equation [Ref. 5, chap. 7. Eq. (7.26)], the phase noise is given as

$$L(f_m) = 10\log \left\{ \left[1 + \frac{f_0^2}{(2f_m Q_L)^2(1-m)^2} \right] \left(1 + \frac{f_c}{f_m} \right) \frac{FkT}{2P_0} + \frac{2kTRK_0^2}{f_m^2} \right\} \tag{156}$$

$$L(f_m) = 10\log \left\{ \left[1 + \frac{f_0^2}{(2f_m Q_0)^2 m^2(1-m)^2} \right] \left(1 + \frac{f_c}{f_m} \right) \frac{FkT}{2P_0} + \frac{2kTRK_0^2}{f_m^2} \right\} \tag{157}$$

where $m = \frac{Q_L}{Q_0}$

From [Ref. 5, Eq. 10.317], the minimum phase noise can be found by differentiating Eq. (157) and equating to zero as $\frac{\partial}{\partial m}[£(f_m)]_{m=m_{\text{opt}}} = 0$:

$$\frac{d}{dm}\left[10\log \left\{ \left[1 + \frac{f_0^2}{(2f_m Q_0)^2 m^2(1-m)^2} \right] \left(1 + \frac{f_c}{f_m} \right) \frac{FkT}{2P_0} + \frac{2kTRK_0^2}{f_m^2} \right\} \right] = 0 \Rightarrow m_{\text{opt}} \approx 0.5 \tag{158}$$

Figure 51 shows the plot of the relative phase noise versus the ratio between loaded and unloaded Q factor of the resonator (e.g., [Ref. 5, Appendix C]).

Figure 50 Small signal model of the grounded base oscillator [5] (Rohde et al. [5]/John Wiley & Sons).
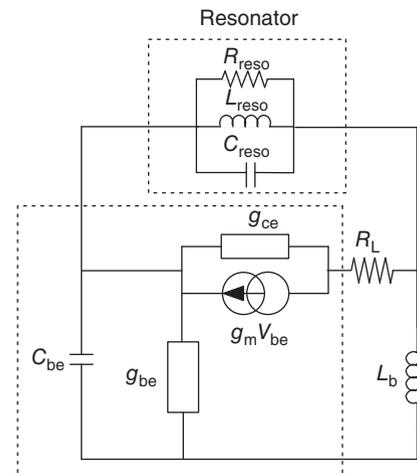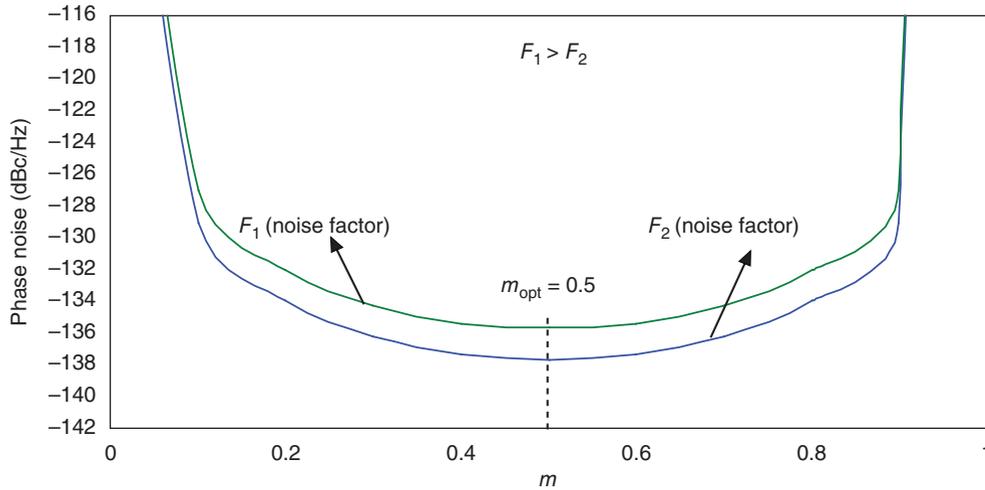
Figure 51 Relative phase noise versus the ratio of loaded and unloaded Q of the resonator for noise factor F_1 and F_2, ($F_1 > F_2$) (Rohde et al. [5]/John Wiley & Sons).

This implies that for low-noise wideband application, the value of m should be dynamically controlled over the tuning range and it should lie in the vicinity of m_{opt} for ultralow phase-noise performance over the frequency band [43].

12.3 Push–Push Configuration

Figure 52 shows the two identical oscillator circuits coupled through the arbitrary coupling network under push–push configuration.

The evaluation of pushing factor of the push–push configuration is carried out by considering uncorrelated noise voltage perturbation, Δv_{n1} and Δv_{n2}, associated with the two identical oscillator circuits as shown in Fig. 52. From [5, 44, 45], due to the symmetry of the push–push oscillator topology, two-modes [common and differential mode (DM)] exist and the corresponding pushing factor is calculated in terms of the common mode (CM) and DM pushing factor.

The frequency noise spectral density for the push–push topology can be given by

$$\left[\overline{\Delta f_n^2}\right]_{\text{push–push}} = ([\Delta f_n]_{\text{CM}} + [\Delta f_n]_{\text{DM}})^2 \tag{159}$$

$$\left[\overline{\Delta f_n^2}\right]_{\text{push–push}} = [K_{\text{PF}}]_{\text{CM}}^2 \left[\overline{\Delta v_n^2}\right]_{\text{DM}} + [K_{\text{PF}}]_{\text{DM}}^2 \left[\overline{\Delta v_n^2}\right]_{\text{DM}} + 2[K_{\text{PF}}]_{\text{CM}}[K_{\text{PF}}]_{\text{DM}}([\Delta v_n]_{\text{CM}} * [\Delta v_n]_{\text{DM}}) \tag{160}$$

where $[K_{\text{PF}}]_{\text{CM}}$ and $[K_{\text{PF}}]_{\text{DM}}$ are common and DM pushing factors, and $[\Delta v_n]_{\text{CM}}$ and $[\Delta v_n]_{\text{DM}}$ are the common and DM noise perturbations.

The effect of the differential noise perturbation, due to the symmetry for the push–push topology, gives an insignificant variation of the oscillating frequency, so $[K_{\text{PF}}]_{\text{DM}} \to 0$.

The CM input noise perturbation of the circuit (shown in Fig. 3c) can be given as

$$\left[\overline{\Delta v_n^2}\right]_{\text{CM}} = \left[\overline{\frac{\Delta v_{n1} + \Delta v_{n2}}{2}}\right]^2 = \frac{1}{4}\left(\left[\overline{\Delta v_{n1}^2}\right] + \left[\overline{\Delta v_{n2}^2}\right] + \left[\overline{\Delta v_{n1} * \Delta v_{n2}}\right]\right) \tag{161}$$
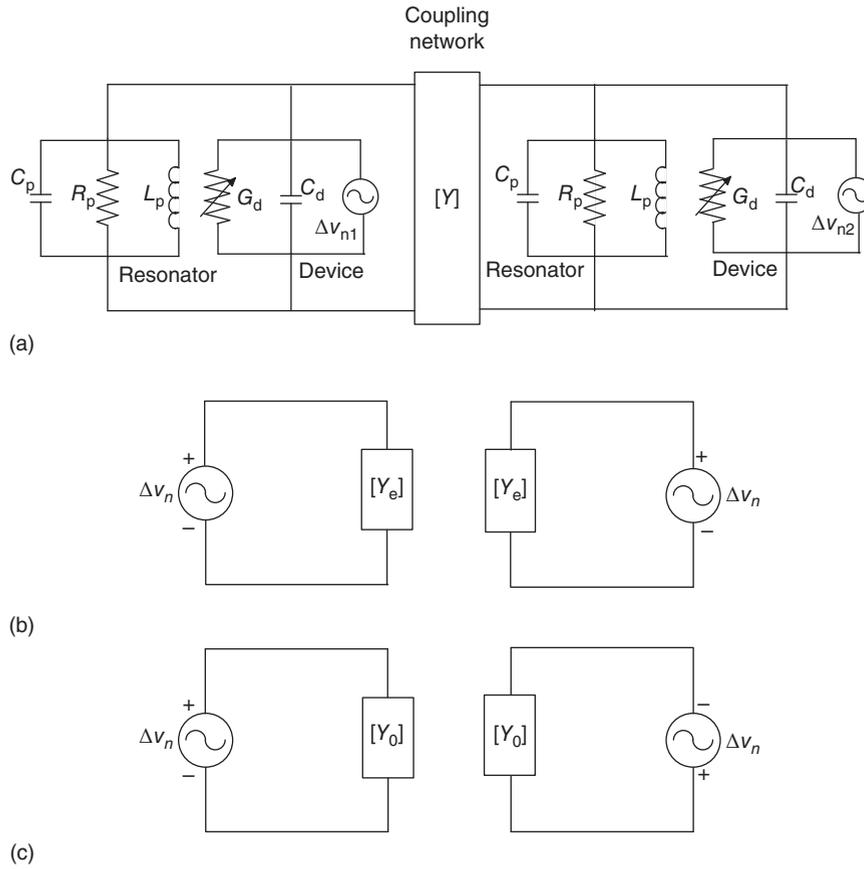
Figure 52 Two identical oscillator circuits coupled through the arbitrary coupling network under push–push configuration. (a) Push–push configuration. (b) Common mode (CM): $\Delta v_{n1} = \Delta v_{n2} = \Delta v_n$. (c) Differential mode (DM): $\Delta v_{n1} = -\Delta v_{n2} = \Delta v_n$ (Rohde et al. [5]/John Wiley & Sons).

Since the input noise voltage perturbation Δv_{n1} and Δv_{n2} associated with the two identical active devices are uncorrelated to each other, $[\overline{\Delta v_{n1} * \Delta v_{n2}}] = 0$. Considering the active device (transistor) for the two identical oscillator circuits in push–push topology operates under the same working condition, their input noise voltage perturbation can be described by the same statistic and given as $\left[\overline{\Delta v_{n1}^2}\right] = \left[\overline{\Delta v_{n2}^2}\right]$.

Equation (161) can be rewritten as

$$\left[\overline{\Delta V_n^2}\right]_{\text{CM}} = \left[\frac{\Delta v_{n1} + \Delta v_{n2}}{2}\right]^2 = \left[\frac{\overline{\left[\Delta v_n^2\right]}}{2}\right] \tag{162}$$

From (160),

$$\left[\overline{\Delta f_n^2}\right]_{\text{push–push}} = [K_{\text{PF}}]_{\text{CM}}^2 \left[\overline{\Delta v_n^2}\right]_{\text{CM}} = [K_{\text{PF}}]_{\text{CM}}^2 \left[\frac{\overline{\left[\Delta v_n^2\right]}}{2}\right] \tag{163}$$

From Ref. 5, Eqs. (10.207), (10.208), and (10.222),

$$[L\,(f_m)]_{\text{push}-\text{push}(f=f_0)} = 20\log\left\{\frac{[\Delta f_n]_{\text{push}-\text{push}}}{\sqrt{2}f_m}\right\} = -3\text{ dB} + 20\log\left\{\frac{[K_{\text{PF}}]_{\text{CM}}\Delta v_n}{\sqrt{2}f_m}\right\} \quad (164)$$

From (164), there is a 3 dB improvement in the phase noise with respect to the individual oscillator oscillating at half the frequency of the push–push frequency, and the analysis agrees with the general equation of the N-coupled oscillator described by Ref. 5, Eq. (10.206).

The improvement of the phase noise of the push–push topology, referring to one individual oscillator which oscillates at fundamental frequency f_0, can be expressed as

$$\frac{[L\,(f_m)]_{\text{push}-\text{push}(f=f_0)}}{[L\,(f_m)]_{\text{fundamental}\left(f=2\frac{f_0}{2}\right)}} = \frac{20\log\left\{\frac{[\Delta f_n]_{\text{push}-\text{push}(f=f_0)}}{\sqrt{2}f_m}\right\}}{20\log\left\{\frac{[\Delta f_n]_{\text{fundamental}\left(f=2\frac{f_0}{2}\right)}}{\sqrt{2}f_m}\right\}} \quad (165)$$

From Ref. 5, Eqs. (10.208) and (10.217),

$$[L\,(f_m)]_{\text{push}-\text{push}(f=f_0)} = -9\text{ dB} + [L\,(f_m)]_{\text{fundamental}\left(f=2\frac{f_0}{2}\right)} \quad (166)$$

where $f_0/2$ is the fundamental frequency of the sub-circuit of the oscillator in push–push topology.

From (166), push–push topology gives 9 dB improvement in the phase noise compared to the fundamental frequency of the individual oscillator oscillating at f_0, twice the designed oscillating frequency of $f_0/2$.

The above relative noise analysis gives a theoretical basis of the noise prediction as [46]:

- *Fundamental Oscillator*. 12 dB degradation of the phase noise with respect to the fundamental oscillator oscillating at f_0, twice the designed oscillating frequency $f_0/2$.
- *Frequency Multiplier/Doubler*. 6 dB degradation of the phase noise with respect to the fundamental oscillator oscillating at f_0, twice the designed oscillating frequency of $f_0/2$.
- *Push–push topology (f = 2f_0/2)*. 9 dB improvement of the phase noise with respect to the fundamental oscillator oscillating at f_0, twice the designed oscillating frequency of $f_0/2$.

12.4 Validation

Figure 53 shows the schematic of the push–push oscillator that has two identical oscillators. It consists of two individual oscillators that are oscillating at half the push–push frequency ($f_0/2$). The individual oscillator, corresponding to the half-resonator, oscillates at $f_0/2$ (1000 MHz) and is used as a starting point to verify the above noise analysis with respect to the frequency multiplier and push–push configuration.

Figure 53 shows the phase-noise plot of the individual oscillator operating at a fundamental frequency of $f_0/2$ (1000 MHz) and f_0 (2000 MHz), working as a frequency doubler (frequency multiplier) at 2000 MHz and a push–push configuration at 2000 MHz.

As discussed above, the phase noise of the fundamental oscillator operating at double the oscillating frequency 2000 MHz is worsening by 12 dB/octave with respect to the fundamental oscillator oscillating at a frequency of 1000 MHz.

The simulated graph is based on the unchanged parameters of the active device and the passive components with respect to the two-frequency $f_0/2$ and f_0. It is not an easy task to design the same oscillator operating at $f_0/2$ and f_0 and maintain the same operating parameters of the active device, coupling coefficient, drive level, quality factor, etc.

For the case of the frequency doubler, the phase noise is degraded by 6 dB with respect to the fundamental frequency as shown in Fig. 54.
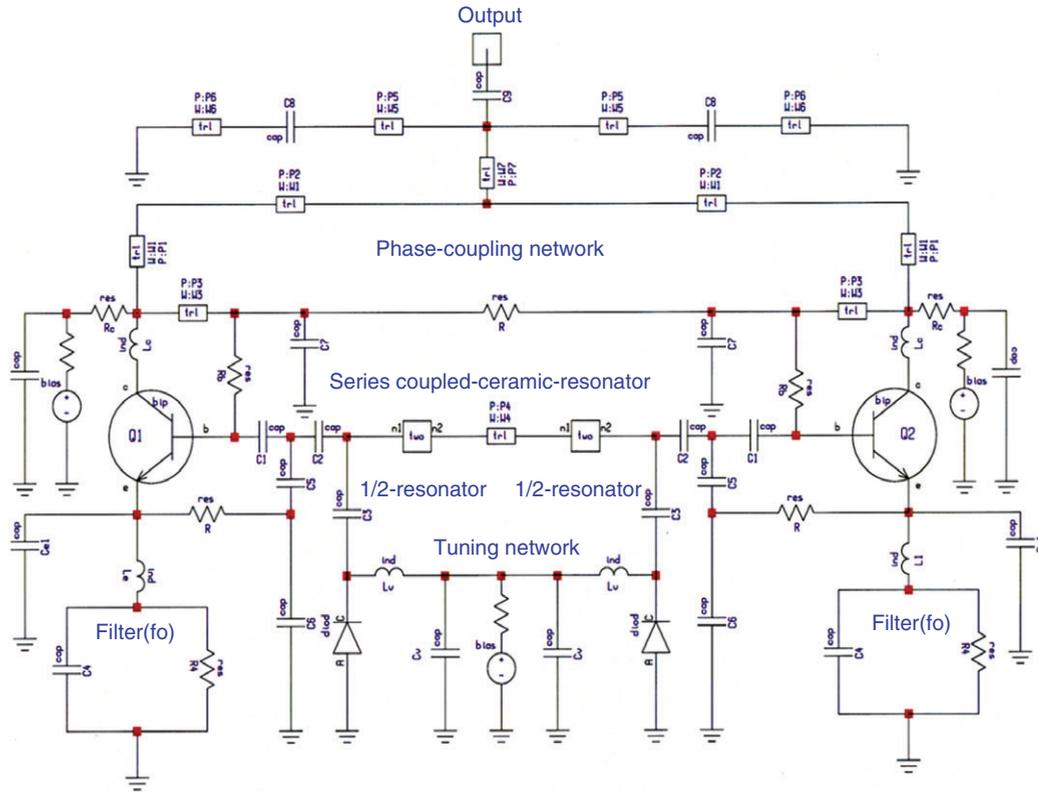
Figure 53 Schematic of the push–push oscillator (Rohde et al. [5]/John Wiley & Sons).
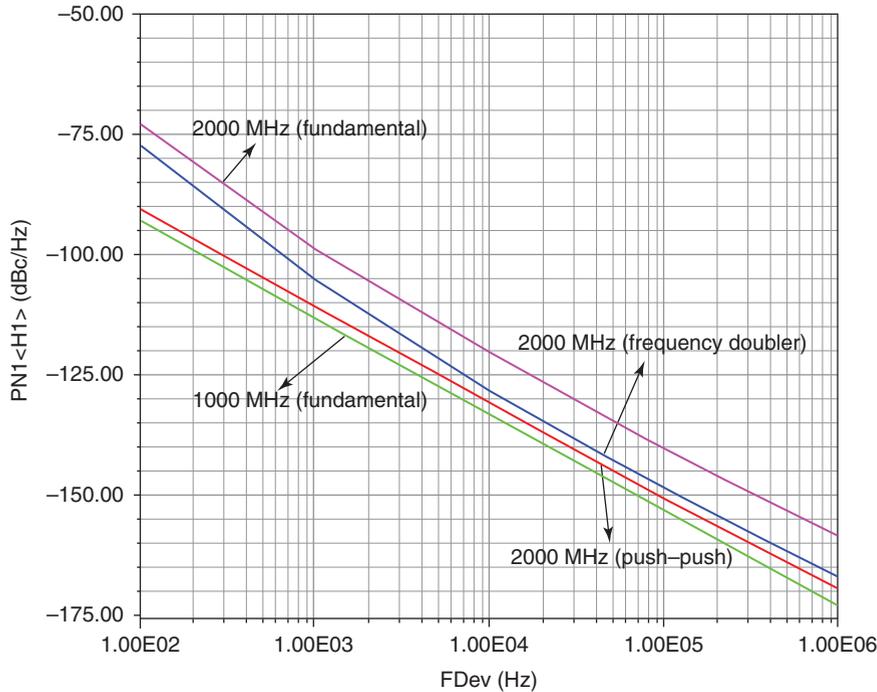
Figure 54 Phase-noise plot of fundamental oscillator at $f_0/2$, and f_0, frequency doubler at f_0, and push–push oscillator at f_0 (Rohde et al. [5]/John Wiley & Sons).

R&S FSUP 26 Signal Source Analyzer		Locked

Figure 55 Measured phase-noise plot of 7680 MHz.

Measurement complete

Date: 8.OCT.2014   17 : 10 : 48

Grün: Ref-640-MHz

Schwarz: Ref-7680-MHz

The relative improvement of the phase noise of the push–push configuration, with respect to the fundamental frequency of the oscillator composed of push–push topology, is 9 dB. This is shown in Fig. 54 and agrees with the theoretically predicted result [5, 46].

Figure 55 shows the phase noise of a phase locked loop (PLL), green trace uses a 640 MHz reference and the black trace uses a 7680 MHz reference. The reason why the black curve is noisier is because the reference frequency is much higher. If the push–push oscillator of Fig. 53 is part of a PLL circuit, the phase noise improves. The green curve shows a reference frequency of 640 MHz and the black curve shows a reference frequency of 7680 MHz (and is noisier because of the higher operating frequency of the phase frequency discriminator).

Figure 56 shows the measured phase noise of the push-push free running oscillator of Fig. 53. The plot shows the phase noise over the entire tuning range.

Figure 57 shows the typical phase noise of some typical phase-noise values for modern synthesized signal generators.

Figure 56 Measured phase-noise plot of 7680 MHz.

Figure 57 Some typical phase-noise values for modern synthesized signal generators (R&S).
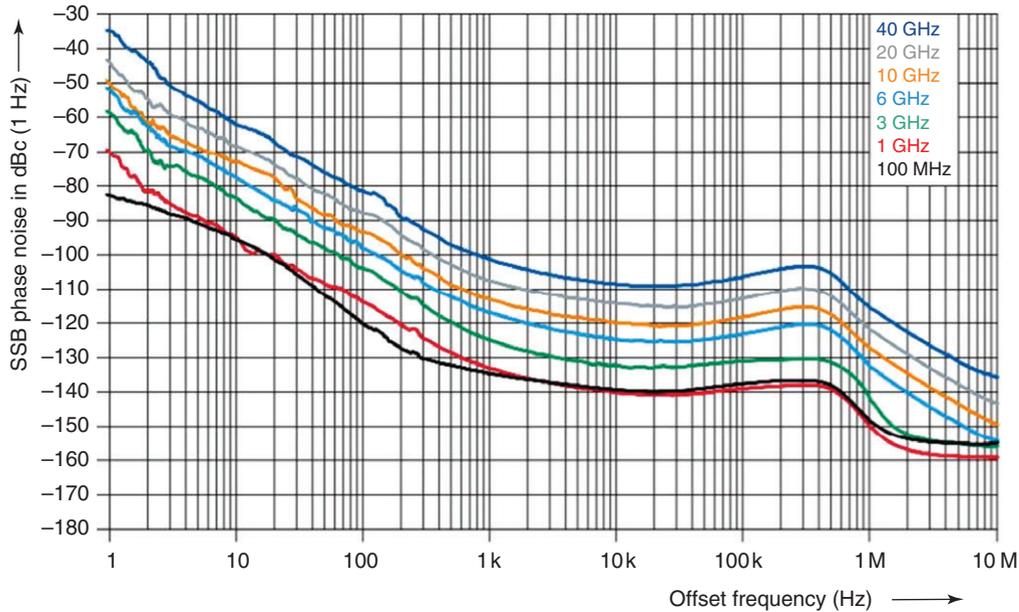
Figure 58 Comparison of phase-noise values for different frequencies from the same signal generator (Courtesy Rohde and Shwarz).

Figure 58 shows Phase noise of the different frequencies from the same signal generator (R&S SMA 100B) [Courtesy R&S].

13 2400 MHz MOSFET-BASED PUSH–PULL OSCILLATOR

Wireless applications are extremely cost sensitive, and when implemented as an RFIC, they are designed using silicon technology. Most mixers in RFIC's are built on the principle of differential amplifiers (Gilbert cell) and require a phase and out-of-phase signal (symmetrical drive). For these symmetrical requirements, this is best achieved using a push–pull technology with two outputs. The design choices are SiGe transistors or bipolar CMOS (BiCMOS) transistors. The submicron devices in 0.35-micron technology and smaller are ideally suited for this frequency application. The 0.25 and smaller technology is more costly but does not provide a significant advantage. As will be seen, the critical phase noise is determined by the Q of the inductor and other elements of the resonator and by the flicker noise from the device.

Figure 59 shows the circuit of the 2400 MHz integrated CMOS oscillator 0.35 μm in cross-coupled (push–pull) configuration [47–66].

The circuit above uses a cross-coupled CMOS–NMOS pair as an oscillator. The advantage compared to an all-NMOS structure is that it generates a large symmetrical signal swing and balances out the pull-up and pull-down signals, resulting in a better noise. This type of topology rejects the CM noise and substrate noise.

Figure 60 shows the starting condition which requires a negative resistance and a cancellation of the reactances at the frequency of oscillation. The currents shown in Fig. 61 indicate that this condition is met.

It is important to notice that the condition of zero reactance does not quite occur at the point of most negative current. Since the circuit is totally symmetrical, only the condition $C_1 = C_2$ can be met [Ref. 5, Section 8.6]. C_1 and C_2 refer to the gate source capacitance of the field-effect transistors. As outlined previously, this is not necessarily the best condition for phase noise.

Figures 61 and 62 show the predicted phase and RF output power, including harmonic contents.
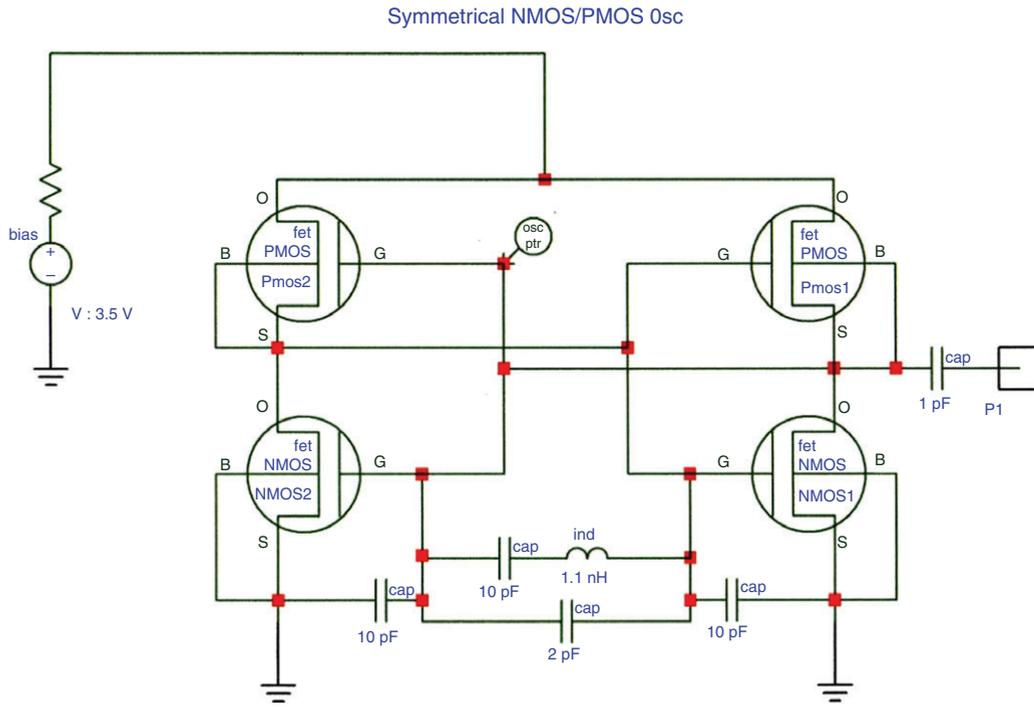
Figure 59 Circuit of the 2400 MHz integrated CMOS oscillator (Rohde et al. [5]/John Wiley & Sons).
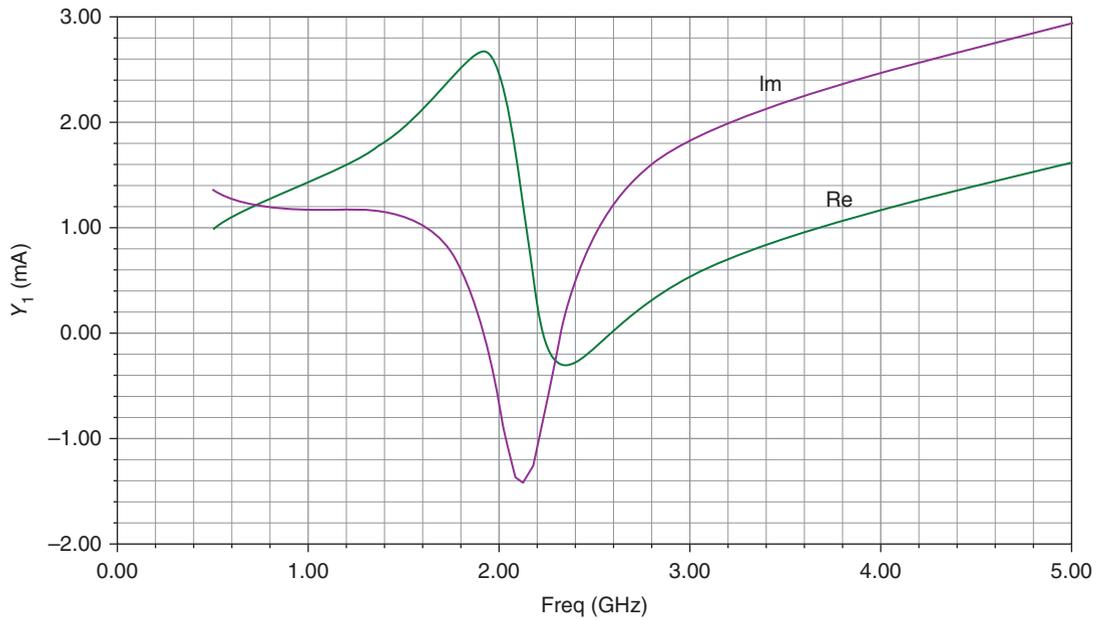
Figure 60 The real and imaginary currents that cause the negative resistance for oscillation (Rohde et al. [5]/John Wiley & Sons).
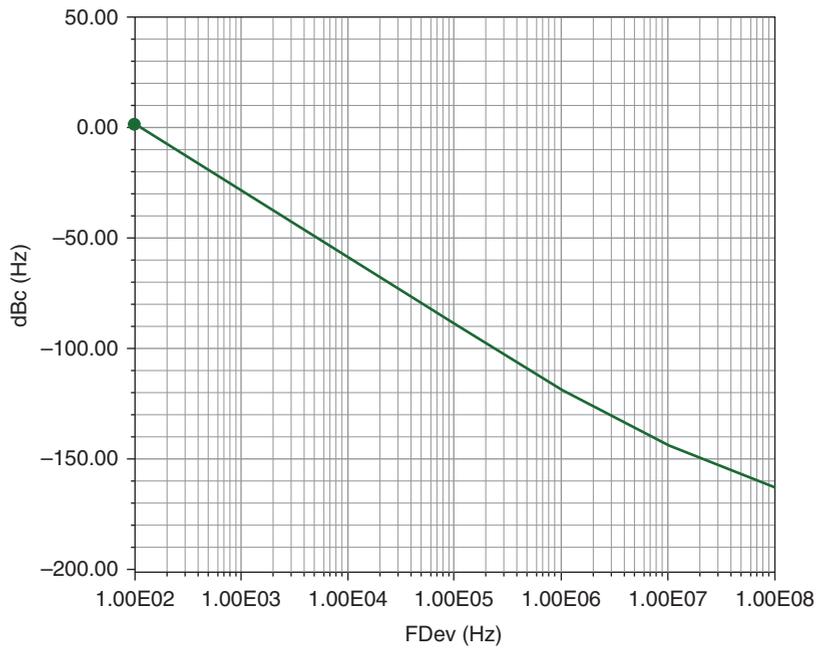
Figure 61 Predicted phase noise of the 2400 MHz MOSFET [5] oscillator (Rohde et al. [5]/John Wiley & Sons).
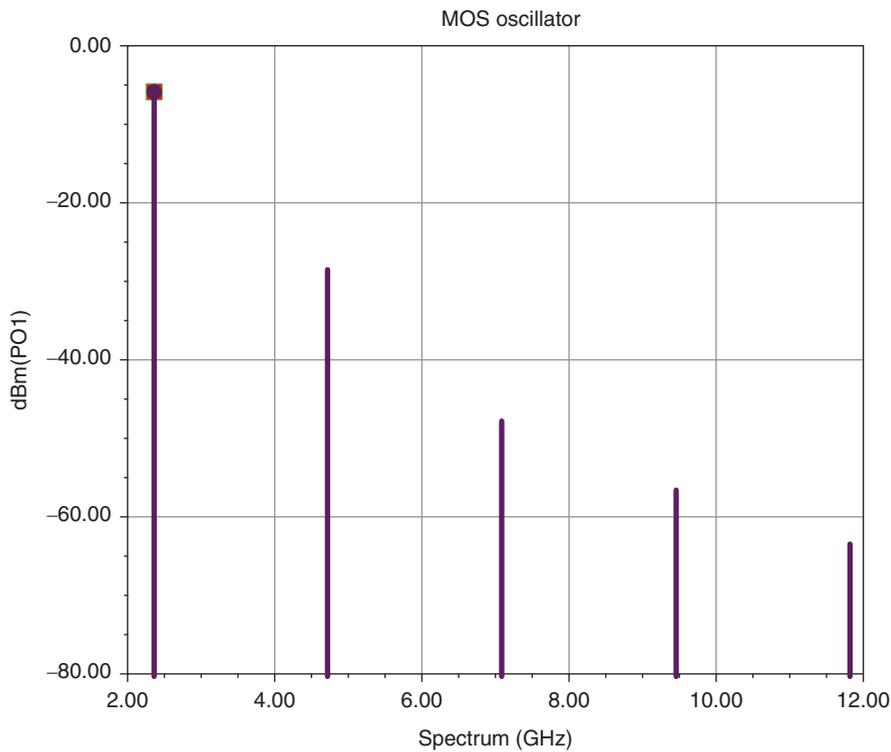
Figure 62 Predicted output spectrum of the 2400 MHz MOSFET oscillator (Rohde et al. [5]/John Wiley & Sons).

Figure 63 Determining the transconductance of the differential circuit of the cross-coupled PMOS and NMOS pair (Rohde et al. [5]/John Wiley & Sons).
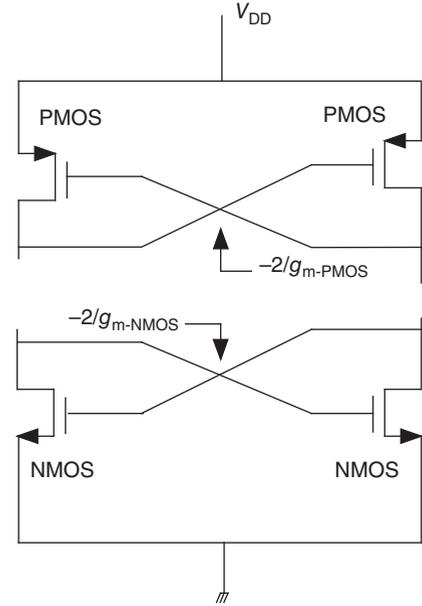
13.1   Design Equations

1. The transconductance

Figure 63 shows a cross-coupled P-type MOS (PMOS) and a cross-coupled N-type MOS (NMOS) pair using CMOS devices.

According to the literature, PMOS transistors offer lower $1/f$ and thermal noise while NMOS transistors exhibit a higher f_T and a higher transconductance for the same operating point.

The total transconductance is

$$[g_m]_{\text{large-signal}} = -\frac{[g_m]_{\text{PMOS}} + [g_m]_{\text{NMOS}}}{2} \tag{167}$$

$$[g_m]_{\text{large-signal}} = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{168}$$

$$[g_m]_{\text{NMOS}} = \sqrt{2 I_{ds} \mu_{\text{NMOS}} C_{\text{ox-NMOS}} \left[\frac{w}{L}\right]}_{\text{NMOS}} \tag{169}$$

$$[g_m]_{\text{PMOS}} = \sqrt{2 I_{ds} \mu_{\text{PMOS}} C_{\text{ox-NMOS}} \left[\frac{w}{L}\right]}_{\text{PMOS}} \tag{170}$$

$$\frac{\partial I_{ds}}{\partial V_{gs}} = K_p \frac{\omega}{L}(V_{gs} - V_{th}) \tag{171}$$

$$[g_m]_{\text{large-signal}} = \sqrt{\frac{2 w K_p I_{ds}}{L}} \tag{172}$$

with

K_p is the transconductance parameter;

μ_{PMOS} is the carrier mobility of the PMOS device;

μ_{NMOS} is the carrier mobility of the NMOS device;

C_{ox} is the unit capacitance of the gate oxide.

2. The transconductance parameter

The transconductance parameter is defined as

$$K_p = \mu C_{\text{ox}} \tag{173}$$

where μ is the carrier mobility and C_{ox} is the unit capacitance of the gate oxide.

3. The gate-oxide capacitance of the device

The unit capacitance of the gate oxide C_{ox} is given as

$$C_{\text{ox}} = \varepsilon_{\text{ox}} \left[\frac{w_i l_i}{t_{\text{ox}}} \right] \tag{174}$$

with

ε_{ox} is the permittivity of the oxide;
t_{ox} is the thickness of the oxide layer between spiral and substrate;
w_i is the width of the spiral line;
l_i is the length of the spiral line.

4. The drain current

The drain current is

$$I_{ds} = \frac{1}{2} \left[K_p \frac{w}{L} (V_{gs} - V_{th})^2 \right] \tag{175}$$

$$I_{ds} = \frac{g_m}{2} (V_{gs} - V_{th}) \tag{176}$$

where $(V_{gs} - V_{th})$ is defined as

$$(V_{gs} - V_{th}) = \sqrt{\frac{2 I_{ds} L}{K_p w}} \tag{177}$$

5. The size of the device

The size of the device determines the transconductance of the transistor and the large-signal transconductance needs to be large enough to sustain oscillation and compensate the losses of the resonator.

The expression of the ratio of the channel width (gate) and channel length (gate) is

$$\frac{w}{L} = \frac{(2SG_P)^2}{2K_p I_{ds}} \rightarrow \frac{(g_m)^2}{2K_p I_{ds}} \tag{178}$$

where w is the width of the channel (gate) and L is the length of the channel (gate) of the device.

6. The total equivalent resistance at resonant frequency

Figures 64a,b shows the equivalent cross-coupled oscillator resonant circuit and the corresponding equivalent resistances at resonance condition.

The total equivalent parallel resistor at resonance frequency is

$$R_T = \frac{2R_P}{2 - R_P(g_{m\text{-NMOS}} + g_{m\text{-PMOS}})} \tag{179}$$

$$Q_L = \frac{R_P}{\omega L} \tag{180}$$

where $g_{m\text{-NMOS}}$ and $g_{m\text{-PMOS}}$ are the corresponding large-signal transconductances of the NMOS and PMOS device.
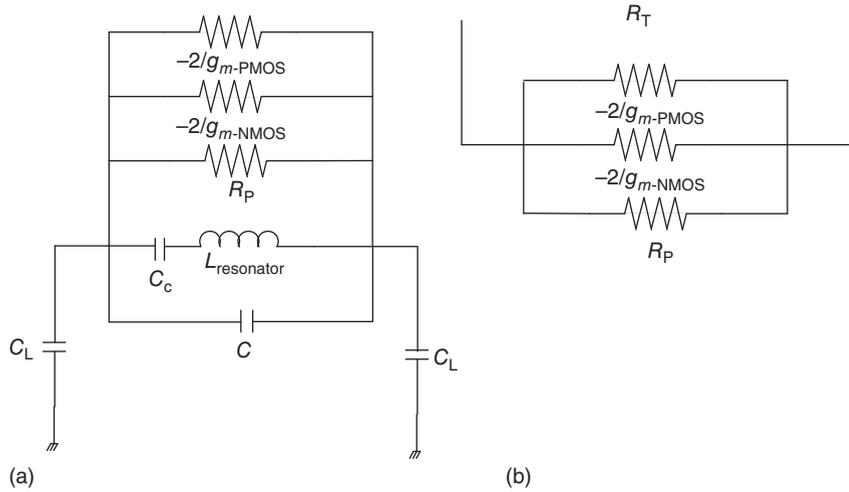
Figure 64 (a) The equivalent cross-coupled oscillator resonator circuit and (b) the equivalent resistances at resonance condition (Rohde et al. [5]/John Wiley & Sons).

For a symmetrical output signal, the large-signal transconductance of the NMOS and PMOS transistors has to be ideally equal as $g_{m\text{-NMOS}} = g_{m\text{-PMOS}} = g_m$ and the equivalent resistance at resonance condition is

$$R_T = \frac{1}{\left[\frac{1}{R_p} - g_m\right]} \tag{181}$$

The differential negative resistance generated by the cross-coupled NMOS and PMOS transistors-pair compensates the parallel loss resistance R_P of the resonator circuit.

7. Start-up conditions

For the start-up condition and guaranteed sustained oscillation condition, the value of R_T must be negative and

$$R_T = \frac{1}{\left[\frac{1}{R_p} - g_m\right]} < 0 \Longrightarrow g_m > \frac{1}{R_p} \tag{182}$$

From the loop gain criteria using a stability factor of 2 (loop gain = 2, the gain is adjusted to 1 by self-adjusting the conducting angle of the circuit), the start-up condition is

$$\frac{g_m}{SG_p} \to 2 \tag{183}$$

where

$$G_P = \frac{1}{R_P} \tag{184}$$

S is the stability factor;
R_P is the equivalent parallel loss resistance of the resonator.

13.2 Design Calculations

13.2.1 Parallel Loss Resistance of the Resonator
The equivalent parallel loss resistance of the resonator is given as

$$R_P = (1 + Q^2)R_s \Rightarrow 101R_s \quad \text{for} \ (Q = 10) \tag{185}$$

where R_s is the series loss resistance.

$$[R_P]_{f=2400 \text{ MHz}} = Q\omega L_{\text{ind}} = 190 \ \Omega \tag{186}$$

where $Q = 10$, $L_{\text{ind}} = 1.1$ nH and $G_P = \frac{1}{R_P} \Rightarrow 6.577$ mS

13.2.2 Large-Signal Transconductance

$$[g_m]_{\text{large-signal}} = \sqrt{\frac{2wK_pI_{ds}}{L}} = \sqrt{\frac{2*(250\text{E}-6)*(35.6\text{E}-6)*(14.8\text{E}-3)}{0.35\text{E}-6}} = 27.435 \text{ mS} \tag{187}$$

13.2.3 Size of the Device
The width of the CMOS is given as

$$\frac{w}{L} = \frac{(2SG_P)^2}{2K_pI_{ds}} \rightarrow \frac{(g_m)^2}{2K_pI_{ds}} \tag{188}$$

$$\frac{w}{L} = \frac{(2SG_P)^2}{2K_pI_{ds}} = 714.3 \ \mu\text{m} \tag{189}$$

For $L = 0.35 \ \mu\text{m}$; $w = 250 \ \mu\text{m}$
where
$K_p = 35.6\text{E}-6$;
$I_{ds} = 14.8$ mA;
$G_P = 6.577$ mS;
$S = 2$.

13.2.4 Oscillation Frequency
The frequency of the oscillation is given as

$$f_0 = \frac{1}{2\pi\sqrt{L_{\text{resonator-tank}}C_{\text{resonator-tank}}}} \tag{190}$$

$$C_{\text{resonator-tank}} = \frac{1}{2}[C_{\text{NMOS}} + C_{\text{PMOS}} + C_L + C] \tag{191}$$

where

$$C_{\text{NMOS}} = 4C_{gd\text{-NMOS}} + C_{gs\text{-NMOS}} + C_{db\text{-NMOS}} \tag{192}$$

$$C_{\text{PMOS}} = 4C_{gd\text{-PMOS}} + C_{gs\text{-PMOS}} + C_{db\text{-PMOS}} \tag{193}$$

For the cross-coupled configuration, $C_{\text{NMOS-Pair}}$ is the series combination of the two C_{NMOS} and is given as

$$C_{\text{NMOS-Pair}} = 2C_{gd\text{-NMOS}} + \frac{1}{2}C_{gs\text{-NMOS}} + \frac{1}{2}C_{db\text{-NMOS}} \tag{194}$$

Similarly, $C_{\text{PMOS-Pair}}$ is the series combination of the two C_{PMOS} and is given as

$$C_{\text{PMOS-Pair}} = 2C_{gd\text{-PMOS}} + \frac{1}{2}C_{gs\text{-PMOS}} + \frac{1}{2}C_{db\text{-PMOS}} \tag{195}$$

The capacitance of the resonator is given as

$$C_{\text{resonator-tank}} = \frac{1}{2}[C_{\text{NMOS}} + C_{\text{PMOS}} + C_L + C] \tag{196}$$

where

$C_L = 10$ pF (load capacitance)

$C = \frac{1}{2}$-resonator-parallel capacitance

$$f_0 = \frac{1}{2\pi\sqrt{L_{\text{resonator-tank}}C_{\text{resonator-tank}}}} = \frac{1}{2\pi\sqrt{1.1\text{E}-9 * 3.3\text{E}-12}} = 2400 \text{ MHz} \qquad (197)$$

where

$$L_{\text{resonator-tank}} = 1.1 \text{ nH}, \quad C_{\text{resonator-tank}} = 3.3 \text{ pF}$$

13.2.5 Phase Noise

The phase noise of CMOS oscillators has been subject to endless discussions. The main contributors are still the resonant circuit with a low Q and the flicker frequency contribution from the device. From [Ref. 5, Chapter 8], we take the following equations and adapt them to the CMOS device.

$\text{PN}_{inr}(\omega_0 + \omega) = \frac{4KT}{R_P}[\text{NFT}_{inr}(\omega_0)]^2 = \frac{4KT}{R_P}\left\{\frac{1}{2}\left[\frac{1}{2\omega_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow$ phase-noise contribution from the resonator.

$\text{PN}_{Vgn}(\omega_0 + \omega) = 4KTr_g[\text{NFT}_{Vgn}(\omega_0)]^2 = 4KTr_g\left\{\frac{1}{2}\left[\frac{C_1+C_2}{C_2}\right]\left[\frac{1}{2Q_0}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow$ phase-noise contribution from the gate resistance.

$\text{PN}_{ign}(\omega_0 + \omega) = 2qI_g[\text{NFT}_{ign}(\omega_0)]^2 = 2qI_g\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{\omega_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow$ phase-noise contribution from the gate current.

$\text{PN}_{ign}(\omega_0 + \omega) = \left(\frac{8kT_{gm}}{3} + \frac{K_f I_g^{AF}}{f_m}\right)[\text{NFT}_{ign}(\omega_0)]^2 = \left(\frac{8kT_{gm}}{3} + \frac{K_f I_g^{AF}}{f_m}\right)\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{2\omega_0 Q_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow$ phase-noise contribution from the flicker noise of the transistor.

$\text{PN}_{idn}(\omega_0 + \omega) = 2qI_d[\text{NFT}_{idn}(\omega_0)]^2 = 2qI_d\left\{\frac{1}{2}\left[\frac{C_1}{C_1+C_2}\right]\left[\frac{1}{2\omega_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow$ phase-noise contribution from the drain current.

The following values were used:

$R_p = 190 \ \Omega$

$f_0 = 2.4$ GHz

$L = 1.1$ nH

$C_O = 2$ pF

$C_1 = C_2 = 0.2$ pF

$n = 2$

$I_g = 100 \ \mu\text{A}$

$I_d = 14$ mA

$AF = 2$

$KF = 5\text{E}-5$

$q = 1.6\text{E}-19$

$T = 290$ K

and the following contributions were obtained at 1 MHz offset:

PN1 = −117.78 dBc/Hz

PN2 = −146.37 dBc/Hz

PN3 = −123.4 dBc/Hz

PN4 = −140.9 dBc/Hz

These calculations show that the phase-noise contribution from the tuned circuit dominates and sets the value at −117.78 dBc/Hz.

The circuit was then analyzed using Microwave Harmonica/Ansoft Designer, using a lossy circuit with a Q_0 of 10, and using the SPICE-type parameters which were obtained from the manufacturer.
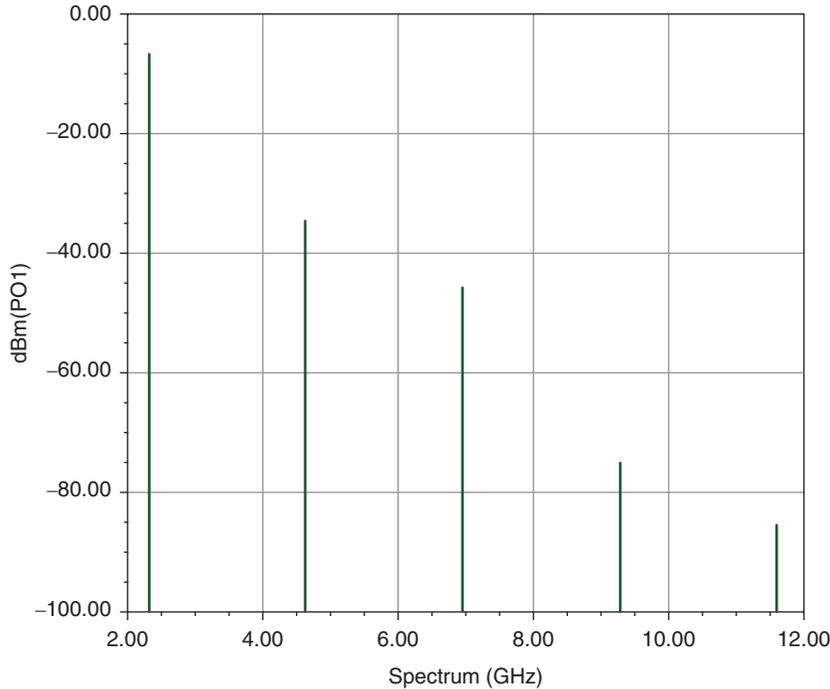
Figure 65 The predicted output spectrum of the CMOS oscillator (Rohde et al. [5]/John Wiley & Sons).

The output power measured single-ended was −7 dBm. Figure 65 shows the simulated output power and harmonic contents. The accuracy of the prediction is within 1 dB.

Figure 66 shows the predicted phase noise from Designer and the phase-noise prediction from the set of equations shown above. It should be pointed out that close-in, the flicker noise contribution dominates, in the medium range, the resonator Q dominates, and, for high currents, the drain current adds significant noise.

This approach has shown a very good agreement between the simulations and calculations as demonstrated. The [Ref. 5, Table 8.1] shows a list of oscillators implemented in various technologies. It is apparent from the list that this design is state of the art. The publications, which cover this topic, have analyzed various other contributions, from both the transistor and the tuning mechanism. When FETs are used as varactors, the average Q is in the vicinity of 30, which means that the low Q inductor still is responsible for the overall phase noise. The three areas of improvement are the power supply voltage, the Q, and the device selection. So far, the power supply voltage has not been addressed; however, latest designs operating at 1.5 V show a poorer noise performance. Their distinct trade-offs and the application dictate if such degradation is allowable.

13.2.6   1/*f* Noise
The electrical properties of surfaces or boundary layers are influenced energetically by states, which are subject to statistical fluctuations and, therefore, lead to the flicker noise or 1/f noise for the current flow.

1/f—noise is observable at low frequencies and generally decreases with increasing frequency f according to the 1/f—law until it will be covered by frequency-independent mechanism, like thermal noise or shot noise.

Example: The noise for a conducting diode is bias dependent and is expressed in terms of AF and KF.

$$\left\langle i_{Dn}^2 \right\rangle_{AC} = 2qI_{dc}B + KF\frac{I_{DC}^{AF}}{f}B \tag{198}$$
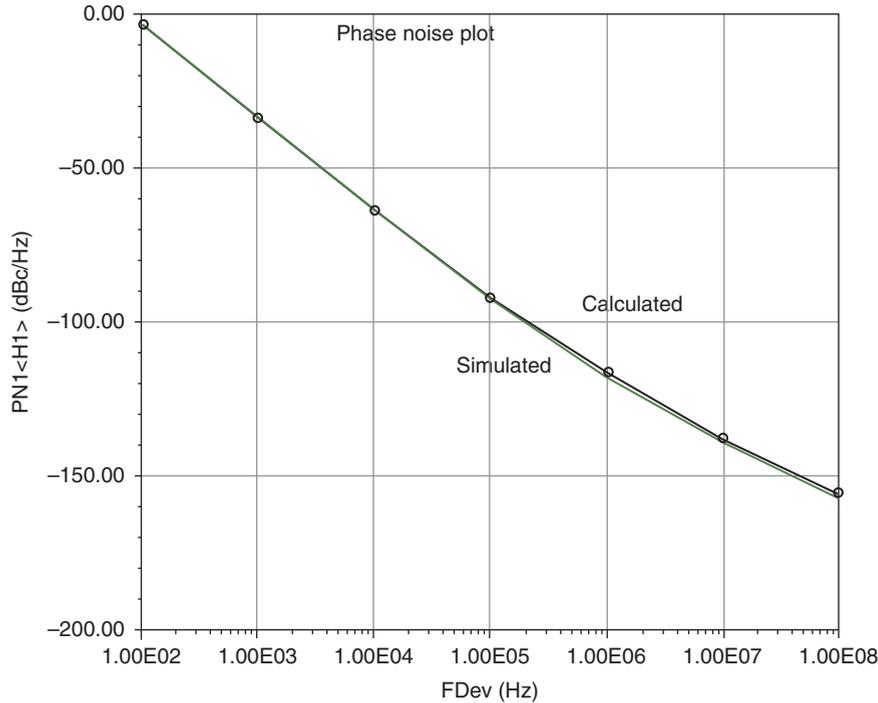
Figure 66 The predicted phase noise from Ansoft Designer (Rohde et al. [5]/John Wiley & Sons).

- The AF is generally in range of 1–3 (dimensionless quantity) and is a bias-dependent curve fitting term, typically 2.
- The KF value is ranging from 10^{-12} to 10^{-6} and defines the flicker corner frequency [32].

One of the important characteristics for device evaluation and selection is $1/f$ noise, which is a function of the active device characteristics and a major contributor to phase noise, especially in applications such as VCOs [5, 20]. In an oscillator, $1/f$ noise that is present in transistors at low frequencies is upconverted and added to the phase noise around the carrier signal. Hence, proper characterization of $1/f$ noise and its effects on phase noise is an important topic. In addition, $1/f$ noise is not solely an active device phenomenon. Passive devices such as carbon resistors, quartz resonators, surface acoustic wave (SAW) devices, and ceramic capacitors are among devices that show the presence of this phenomenon when used as part of low-noise electronic systems. Generally, $1/f$ noise is present in most physical systems and in many electronic components [19, 22, 23].

Flicker noise in BJTs is also known as $1/f$ noise because of the $1/f$ slope characteristics of the noise spectra. This noise is caused mainly by traps associated with contamination and crystal defects in the emitter–base depletion layer. These traps capture and release carriers in a random fashion. The time constants associated with the process produce a noise signal at low frequencies. The flicker noise spectral density is given by

$$S(f)df = (KF)IB^{AF}df/F_c \tag{199}$$

where KF is the flicker noise constant;
AF is the flicker noise exponent;
IB is the DC base current;
F_c is the flicker noise corner frequency.

The measured flicker corner frequency, F_{meas}, is determined by noting the intersection of the $1/f$ noise spectrum and the white noise spectrum. This intersection is where the measured flicker noise power and the white
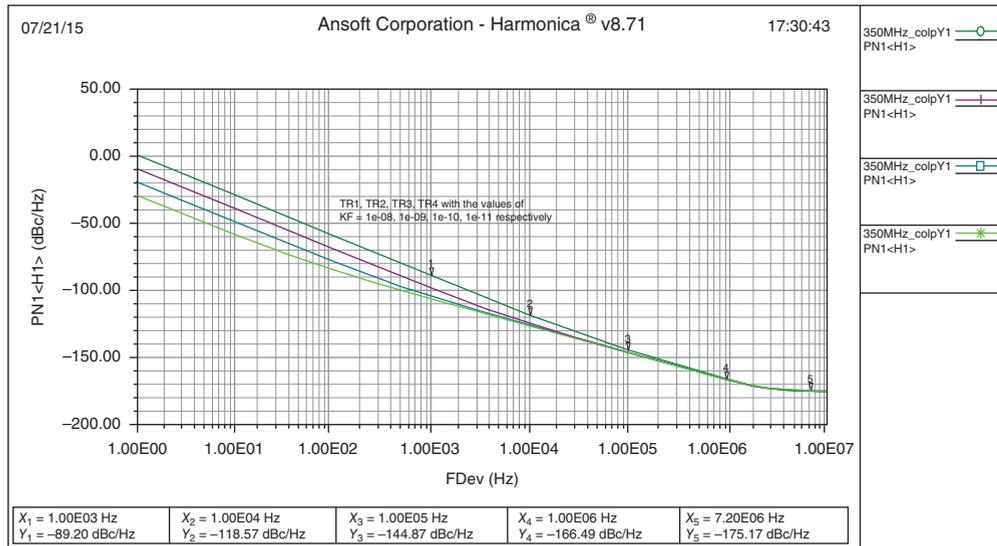
Figure 67 Effect of KF factor on phase noise (Rohde and Apte [33]/IEEE).

noise power are equal. To determine F_{bn}, the intrinsic base flicker noise corner requires solving the following equation [20, 21]:

$$F_{bn} = F_{meas} \left[1 + 1/\beta + 2V_{th}G_{in}/IB \right] \tag{200}$$

where F_{bn} is the intrinsic base flicker noise corner;
F_{meas} is the measured flicker corner;
β is the collector–base current gain;
V_{th} is the thermal voltage $= kT/q$;
G_{in} is the external input conductance;
IB is the DC base biasing current.

The equation for the intrinsic base flicker corner modifies the measured flicker corner to account for the input conductance, base current, and DC current gain of the device. The formula for F_{bn} is valid provided the measured output noise characteristics are dominated by the base flicker and base shot noise sources.

Changing the KF and AF factors affects the phase noise as can be seen from the plots shown in Fig. 67. Y-intercept of the $1/f$ spectra increases proportionally to KF, which is in accordance with Eq. (34). The Y-intercept of the $1/f$ spectra decreases more rapidly with an increase in AF, as seen in Fig. 68. The following discussion of the tuning diodes results in a noise contribution similar to this flicker mechanism.

14 AMPLITUDE MODULATION (AM)-TO-PHASE MODULATION (PM) CONVERSION FROM TUNING DIODES

Figure 69 shows a parallel-tuned circuit which is connected to the oscillator discussed above. The frequency change is obtained by applying a positive voltage to the + terminal. The parallel capacitor is replaced by the two tuning diodes. Here, we will show the influence of the tuning diodes in the voltage-controlled oscillators, the resulting phase noise generated by tuning diodes is shown in Fig. 70.
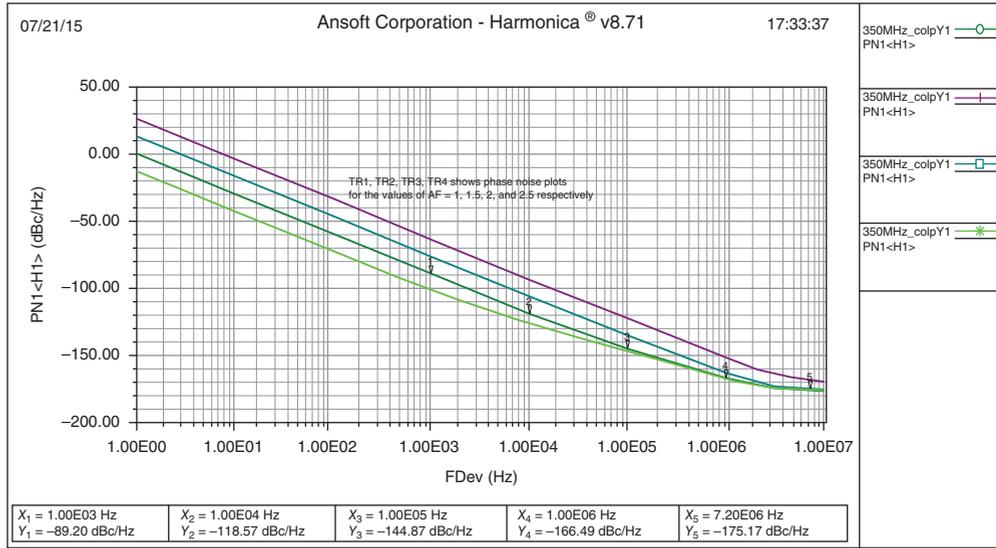
Figure 68 Effect of AF factor on phase noise (Rohde and Apte [33]/IEEE).

Figure 69 Parallel-tuned circuit with tuning diodes (Rohde and Apte [33]/IEEE).
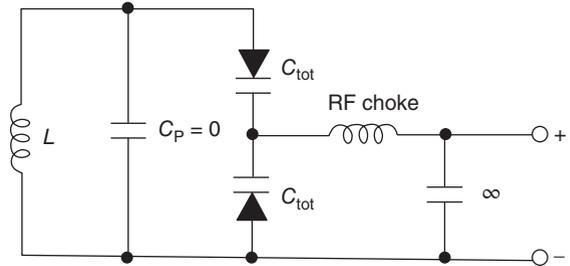
It is possible to define an equivalent noise $R_{a\mathrm{eq}}$ that, inserted in Nyquist's Johnson noise equation,

$$V_n = \sqrt{4kT_oR\Delta f} \tag{201}$$

where $kT_o = 4.2 \times 10^{-21}$ at about 300 K, R is the equivalent noise resistor, and Δf is the bandwidth, which determines an open-circuit noise voltage across the tuning diode. Practical values of $R_{a\mathrm{eq}}$ for carefully selected tuning diodes are in the vicinity of 200 Ω–50 kΩ. If we now determine the noise voltage, $V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 10{,}000}$ the resulting voltage value is 1.296×10^{-8} V$\sqrt{\mathrm{Hz}}$.

This noise voltage generated from the tuning diode is now multiplied with the VCO gain K_o, resulting in the rms frequency deviation

$$(\Delta f_{\mathrm{rms}}) = K_o \times (1.296 \times 10^{-8}\ \mathrm{V})\ \text{in 1-Hz bandwidth} \tag{202}$$

To translate this into an equivalent peak phase deviation,

$$\theta_d = \frac{K_o\sqrt{2}}{f_m}(1.296 \times 10^{-8})\ \text{rad in 1-Hz bandwidth} \tag{203}$$

or for a typical oscillator gain of 100 kHz/V,

$$\theta_d = \frac{0.00183}{f_m}\ \text{rad in 1-Hz bandwidth} \tag{204}$$
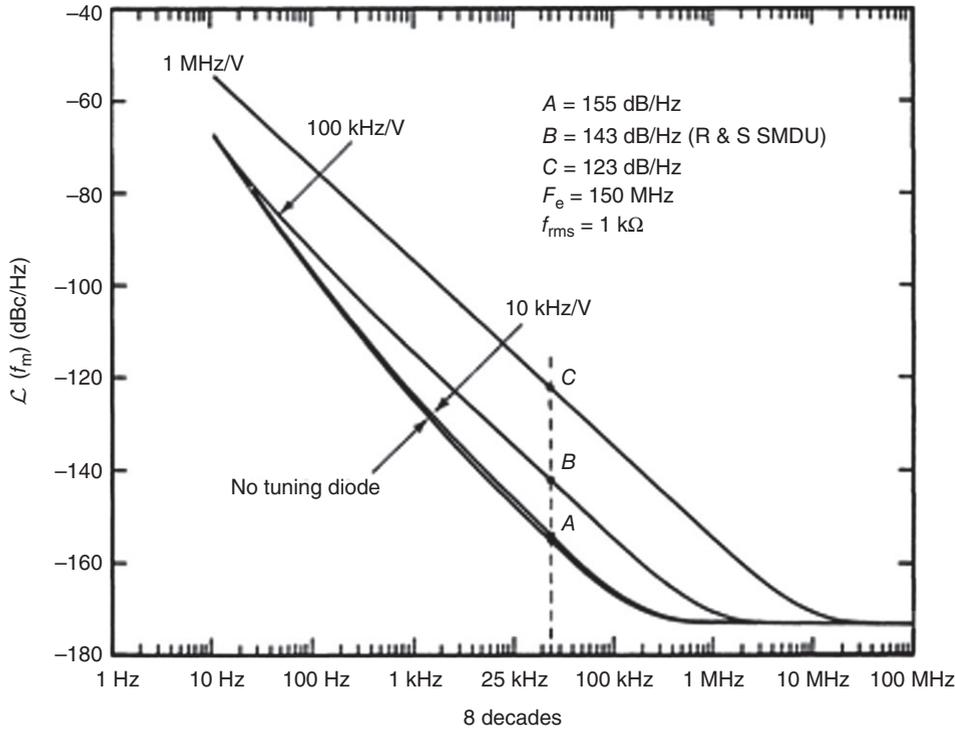
Figure 70   Influence of tuning diode on phase noise (Rohde et al. [5]/John Wiley & Sons).

For $f_m = 25$ kHz (typical spacing for adjacent-channel measurements for frequency modulation (FM) mobile radios), the $\theta_c = 7.32 \times 10^{-8}$. This can be converted now into the single side band (SSB) signal-to-noise ratio:

$$\mathcal{L}(f_m) = 20 \log_{10} \frac{\theta_c}{2} = -149 \text{ dBc/Hz} \tag{205}$$

For the typical oscillator gain of 10 MHz/V found in wireless applications, the resulting phase noise will be 20 dB worse [10 log (10 MHz ÷ 100 kHz)]. However, the best tuning diodes, like the BB104, have an R_n of 200 Ω instead of 10 kΩ, which again changes the picture. Therefore, with $kT_o = 4.2 \times 10^{-21}$, the resulting noise voltage will be

$$V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 200} = 1.833 \times 10^{-9} \text{ V}\sqrt{\text{Hz}} \tag{206}$$

From (72), the equivalent peak phase deviation for a gain of 10 MHz/V in a 1-Hz bandwidth is then

$$\theta_d = \frac{1 \times 10^7 \sqrt{2}}{f_m}(1.833 \times 10^{-9}) \text{ rad} \tag{207}$$

or

$$\theta_d = \frac{0.026}{f_m} \text{ rad in 1-Hz bandwidth} \tag{208}$$

With $f_m = 25$ kHz, $\theta_c = 1.04 \times 10^{-6}$. Expressing this as phase noise:

$$\mathcal{L}(f_m) = 20 \log_{10} \frac{\theta_c}{2} = -126 \text{ dBc/Hz} \tag{209}$$

Figure 70 shows the influence of the tuning diode on the phase noise. For the purpose of discussion, the equivalent noise resistance is assumed 1 kΩ, and three sensitivity curves are shown. For a tuning sensitivity of more

than 100 kHz/V, the varactor noise dominates. As the tuning sensitivity increases, the influence of the oscillator noise itself disappears.

15 SUMMARY

With a systematic approach to the Colpitts oscillator, this paper provides information for an optimized design and the resulting phase noise. Starting with the explanation about the Colpitts oscillator, invented in 1918, we have discussed a linear analysis based on Y-parameters, followed by S-parameter approach, which is applicable to practically all oscillators and then move into the important time-domain analysis. This allows a very reliable design, where the simulated, calculated, and the measured results agree well. This detailed analysis gives a thorough insight into the design approach and results of a Colpitts oscillator. Finally, the noise contribution of the tuning diodes is added. The interested reader, having access to computer aided design (CAD) tools, can run some "experiments" by varying the component values.

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